EVB-LAN9252-DIG-IO

EtherCAT® DIG I/O Evaluation Board User's Guide

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This declaration of conformity is issued by the manufacturer.

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This development/evaluation tool complies with EU RoHS2 Directive 2011/65/EU.

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Derek Carlson
VP Development Tools

12-Sep-14
Date

NOTES:

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Preface

NOTICE TO CUSTOMERS

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Documents are identified with a "DS" number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is "DSXXXXXA", where "XXXXX" is the document number and "A" is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics to open a list of available online help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the EVB-LAN9252-DIG-IO. Items discussed in this chapter include:

- Document Layout
- Conventions Used in this Guide
- The Microchip Web Site
- Development Systems Customer Change Notification Service
- Customer Support
- Document Revision History

DOCUMENT LAYOUT

This document describes how to use the EVB-LAN9252-DIG-IO as a development tool for the Microchip LAN9252 EtherCAT® slave controller. The manual layout is as follows:

- **Chapter 1. "Overview"** – Shows a brief description of the EVB-LAN9252-DIG-IO.
- **Chapter 2. "Board Details & Configuration"** – Includes details and instructions for using the EVB-LAN9252-DIG-IO.
- **Chapter 3. "LAN9252 EEPROM Programming"** – Includes details and instructions for programming the LAN9252 EEPROM.
- **Appendix A. "EVB-LAN9252-DIG-IO Evaluation Board"** – This appendix shows the EVB-LAN9252-DIG-IO.
- **Appendix B. "EVB-LAN9252-DIG-IO Evaluation Board Schematics"** – This appendix shows the EVB-LAN9252-DIG-IO schematics.
- **Appendix C. "Bill of Materials (BOM)"** – This appendix includes the EVB-LAN9252-DIG-IO Bill of Materials (BOM).

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	*MPLAB® IDE User's Guide*
	Emphasized text	...is the *only* compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	*File>Save*
Bold characters	A dialog button	Click **OK**
	A tab	Click the **Power** tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	`#define START`
	Filenames	`autoexec.bat`
	File paths	`c:\mcc18\h`
	Keywords	`_asm, _endasm, static`
	Command-line options	`-Opa+, -Opa-`
	Bit values	`0, 1`
	Constants	`0xFF, 'A'`
Italic Courier New	A variable argument	*`file`*`.o`, where *`file`* can be any valid filename
Square brackets [ ]	Optional arguments	`mcc18 [options]` *`file`* `[options]`
Curly brackets and pipe character: { | }	Choice of mutually exclusive arguments; an OR selection	`errorlevel {0|1}`
Ellipses...	Replaces repeated text	`var_name [, var_name...]`
	Represents code supplied by user	`void main (void) { ... }`

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- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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- **Compilers** – The latest information on Microchip C compilers, assemblers, linkers and other language tools. These include all MPLAB C compilers; all MPLAB assemblers (including MPASM assembler); all MPLAB linkers (including MPLINK object linker); and all MPLAB librarians (including MPLIB object librarian).
- **Emulators** – The latest information on Microchip in-circuit emulators.This includes the MPLAB REAL ICE and MPLAB ICE 2000 in-circuit emulators.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debuggers. This includes MPLAB ICD 3 in-circuit debuggers and PICkit 3 debug express.
- **MPLAB IDE** – The latest information on Microchip MPLAB IDE, the Windows Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB IDE Project Manager, MPLAB Editor and MPLAB SIM simulator, as well as general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include production programmers such as MPLAB REAL ICE in-circuit emulator, MPLAB ICD 3 in-circuit debugger and MPLAB PM3 device programmers. Also included are nonproduction development programmers such as PICSTART Plus and PIC-kit 2 and 3.

CUSTOMER SUPPORT

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- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://www.microchip.com/support

DOCUMENT REVISION HISTORY

DS50002332A (December 2014)

- Initial Release of this Document.

Chapter 1. Overview

1.1 INTRODUCTION

The LAN9252 is a 2-port EtherCAT® slave controller with dual integrated Ethernet PHYs which each contain a full-duplex 100BASE-TX transceiver and support 100Mbps (100BASE-TX) operation. 100BASE-FX is supported via an external fiber transceiver.

Each port receives an EtherCAT® frame, performs frame checking and forwards it to the next port. Time stamps of received frames are generated when they are received. The Loop-back function of each port forwards the frames to the next logical port if there is either no link at a port, if the port is not available, or if the loop is closed for that port. The Loop-back function of port 0 forwards the frames to the EtherCAT® Processing Unit. The loop settings can be controlled by the EtherCAT® master.

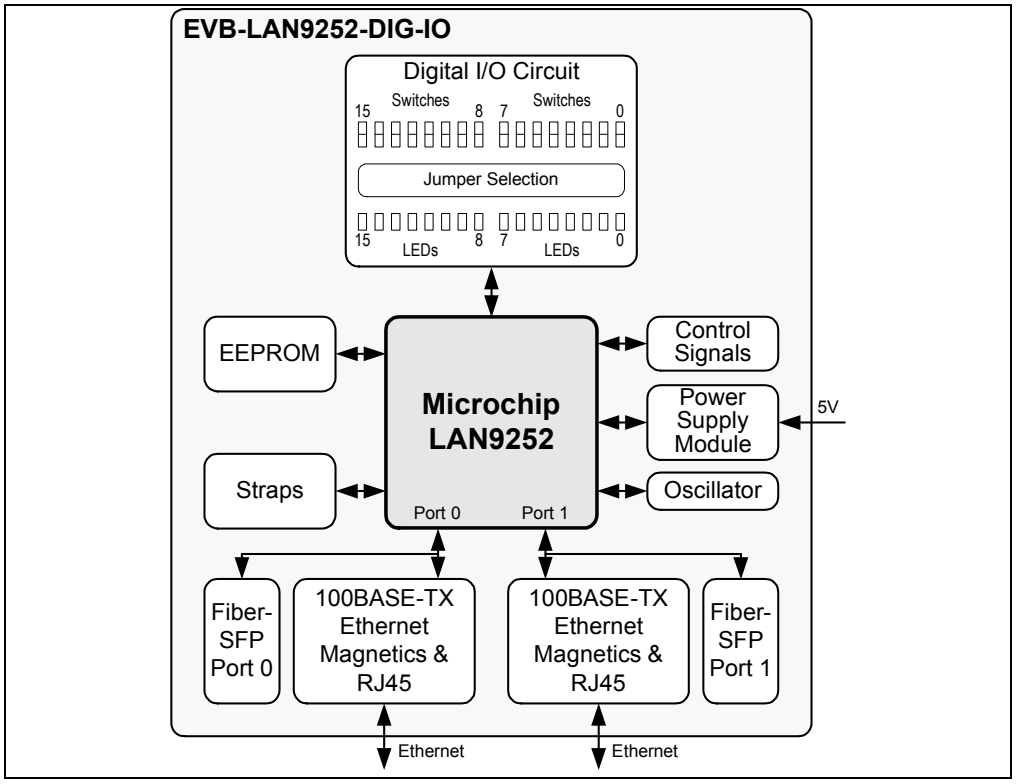
Packets are forwarded in the following order:

Port 0 -> EtherCAT® Processing Unit -> Port 1 -> Port 2.

The EtherCAT® Processing Unit (EPU) receives, analyzes and processes the EtherCAT® data stream. The main purpose of the EtherCAT® Processing unit is to enable and coordinate access to the internal registers and the memory space of the ESC, which can be addressed both from the EtherCAT® master and from the local application. Data exchange between master and slave applications is comparable to a dual-ported memory (process memory), enhanced by special functions for consistency checking (SyncManager) and data mapping (FMMU). Each FMMU performs bitwise mapping of logical EtherCAT® system addresses to physical device addresses.

The scope of this document is to describe the EVB-LAN9252-DIG-IO setup, which supports a Digital I/O Interface and corresponding jumper configurations. The LAN9252 is connected to an RJ45 Ethernet jack with integrated magnetics for 100BASE-TX connectivity. A simplified block diagram of the EVB-LAN9252-DIG-IO is shown in Figure 1-1.

FIGURE 1-1: EVB-LAN9252-DIG-IO BLOCK DIAGRAM



1.2 REFERENCES

Concepts and material available in the following documents may be helpful when reading this document. Visit www.microchip.com for the latest documentation.

- LAN9252 Data Sheet
- AN 8.13 Suggested Magnetics
- EVB-LAN9252-DIG-IO Schematics

1.3 TERMS AND ABBREVIATIONS

IDE - Integrated Development Environment

ESC - EtherCAT® Slave Controller

EVB - Engineering Validation Board

HAL - Hardware Abstraction Layer

HBI - Host Bus Interface

SPI - Serial Protocol Interface

SSC - Slave Stack Code

Chapter 2. Board Details & Configuration

This section includes sub-sections on the following EVB-LAN9252-DIG-IO details:

- Power
- Resets
- Clock
- Configuration
- Mechanicals

2.1 POWER

2.1.1 +5V Power

Power is supplied to the LAN9252 by a +3.3V on-board regulator, which is powered by a +5V external wall adapter (Manufacturer: TRIAD MAGNETICS and P/N: WSU050-3000). The LAN9252 includes an internal +1.2V regulator which supplies power to the internal core logic. Assertion of the D1 Green LED indicates successful generation of +3.3V output. The SW1 switch must be in the ON position for the +5V to power the +3.3V regulator.

2.2 RESETS

2.2.1 Power-on Reset

A power-on reset occurs whenever power is initially applied to the LAN9252 or if the power is removed and reapplied to the LAN9252. This event resets all circuitry within the LAN9252. After initial power-on, the LAN9252 can be reset by pressing the reset switch SW2. The reset LED D2 will assert (red) if when the LAN9252 is in reset condition. For stability, a delay of approximately 180ms is added from the +3.3V output to reset release.

2.2.2 Reset Out

The LAN9252 reset pin can be configured as an output to reset the SoC. The RST# pin becomes an open-drain output and is asserted for the minimum required time of 80ms.

2.2.3 GPIO Reset

The EVB-LAN9252-DIG-IO provides the option to reset the LAN9252 through a PIC GPIO pin [95(RG14)]. The SW10 switch is used for this selection, as shown in Table 2-1.

TABLE 2-1: RESET CONFIGURATION SWITCH

Switch	Short Pins	Knob Position	Function
SW10	1-3	1-2	System Reset (SYS_RST) (Default)
SW10	1-2	1-3	GPIO Reset (GPIO_RST)

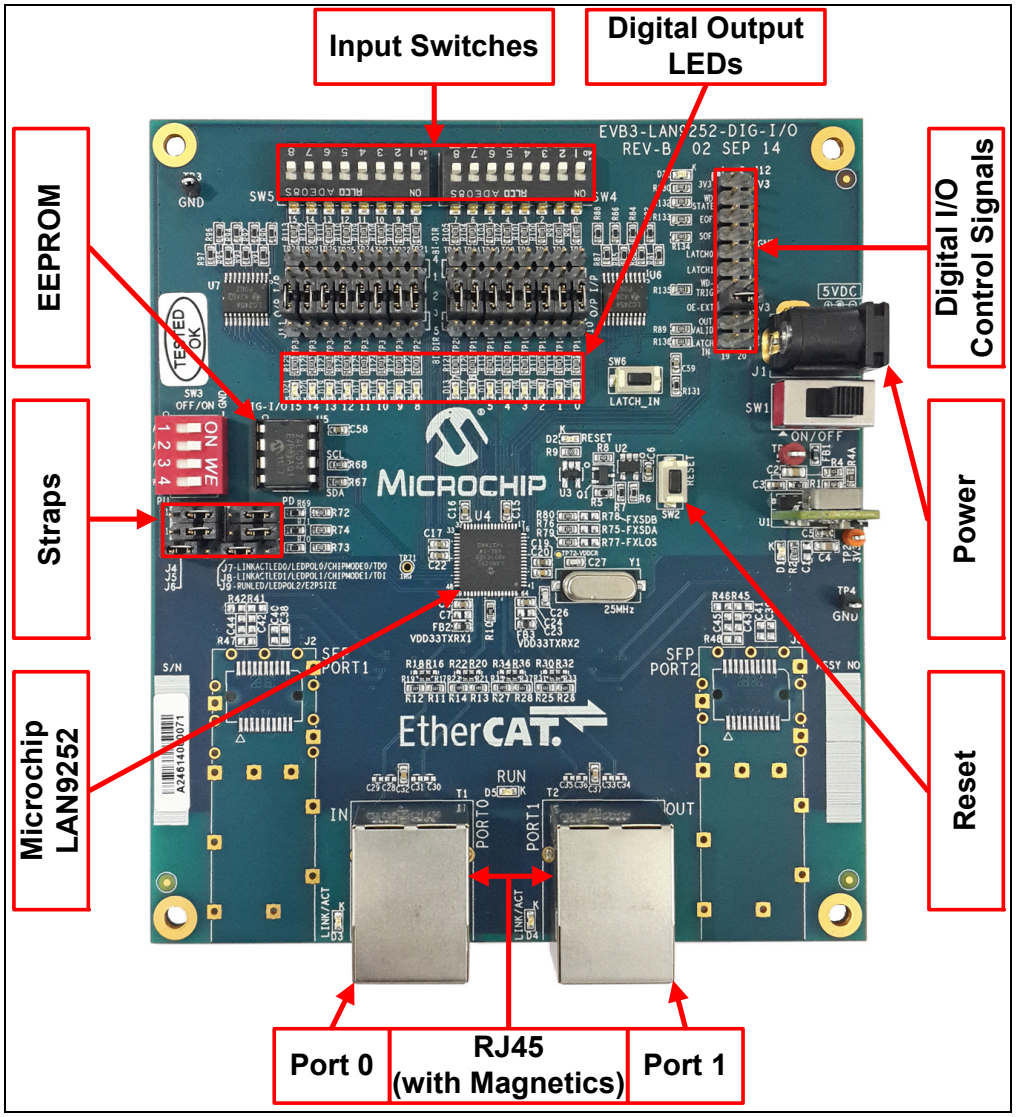
2.3 CLOCK

The EVB-LAN9252-DIG-IO utilizes an external 25Mhz 25ppm crystal from Cardinal Components Inc. (P/N: CSM1Z-A5B2C5-40-25.0D18-F).

2.4 CONFIGURATION

The following sub-sections describe the various board features and configuration settings. A top view of the EVB-LAN9252-DIG-IO is shown in Figure 2-1.

FIGURE 2-1: EVB-LAN9252-DIG-IO TOP VIEW WITH CALLOUTS



2.4.1 Strap Options

2.4.1.1 CHIP MODE SELECTION

Table 2-2 details the LAN9252 chip mode configuration straps.

TABLE 2-2: CHIP MODE CONFIGURATION STRAP

Header	Description	Pins	Settings
J4,J5,J7,J8	Chip mode configuration strap inputs. This strap determines the number of active ports and port types.	1-2 2-3	Short 1-2 for high (pull-up) Short 2-3 for low (pull-down) (default)

Note: For proper operation, chip mode must be in 2-port mode, where Port 0 = PHY A and Port 1 = PHY B. This requires J4, J5, J7, and J8 to be pulled-down (2-3) shorted. All other configurations are not supported by this EVB.

2.4.1.2 EEPROM SIZE CONFIGURATION

The EEPROM size configuration strap (J6 & J9) determines the supported EEPROM size range. A low selects 1Kbits (128 x 8) through 16Kbits (2K x 8)_24C16. A high selects 32Kbits (4K x 8) through 512Kbits (64K x 8) or 4Mbits (512K x 8)_24C512.

TABLE 2-3: EEPROM SIZE CONFIGURATION STRAP

Header	Description	Pins	Settings
J6, J9	EEPROM size configuration strap inputs. This strap determines the supported EEPROM size range.	1-2 2-3	Short 1-2 for high (pull-up) (default) Short 2-3 for low (pull-down)

2.4.1.3 COPPER AND FIBER STRAPS

The LAN9252 supports 100BASE-TX (Copper) and 100BASE-FX (Fiber) modes. In 100BASE-FX operation, the quality of the receive signal is provided by the external transceiver as either an open-drain, CMOS level, Loss of Signal (SFP) or a LVPECL Signal Detect (SFF).

This EVB supports 100BASE-TX (Copper) and SFP 100BASE-FX (Fiber) modes. By default Copper Mode is active. Fiber Mode is supported as an assembly option. To select the Copper or Fiber Mode, the respective strap and signal routing resister assembly options must to be configured.

Note: Vendor part number for SFP: Finisar/FTLF1217P2,
for SFF: Avago Technologies US Inc/AFCT-5971LZ

2.4.1.3.1 Copper Mode

The EVB-LAN9252-DIG-IO is set to Copper Mode by default. Table 2-4 details the required strap resistor settings for Copper Mode operation.

TABLE 2-4: COPPER MODE STRAP RESISTORS

Resistors	Description
R79 (10K)	Configures Port 0 & 1 to Copper Mode
R76, R80 (10K)	Configures Port 0 and Port 1 to Copper Mode, respectively

Note: R75, R77, and R78 must not be populated (DNP).

Additionally, the signal routing resistors detailed in Table 2-5 must be assembled for Copper Mode operation.

TABLE 2-5: COPPER MODE SIGNAL ROUTING RESISTORS

Resistors	Description
R17, R19, R21, R23	Port 0 Copper Mode enabled
R31, R33, R35, R37	Port 1 Copper mode enabled

Note: R16, R18, R20, R22, R30, R32, R34, and R36 (0402 package) must not be populated (DNP).

2.4.1.3.2 Fiber Mode

The EVB-LAN9252-DIG-IO supports SFP type 100BASE-FX. To enabled Fiber Mode, the respective strap and signal routing registers must be configured.

Note: Copper Mode related resistors must be DNP while Fiber Mode is active (See **Section 2.4.1.3.1 "Copper Mode"**).

Table 2-6 details the required strap resistor settings for Fiber Mode operation.

TABLE 2-6: FIBER MODE STRAP RESISTORS

Resistors	Description
R77 (10K)	Configures Port 0 & 1 to FX-LOS Mode
R75, R78 (10K)	Configures Port 0 and Port 1 to Fiber Mode, respectively

Note: R76, R79, and R80 must not be populated (DNP).

Additionally, the signal routing resistors detailed in Table 2-7 must be assembled for Fiber Mode operation.

TABLE 2-7: FIBER MODE SIGNAL ROUTING RESISTORS

Resistors	Description
R16, R18, R20, R22	Port 0 Fiber Mode enabled
R30, R32, R34, R36	Port 1 Fiber mode enabled

Note: R17, R19, R21, R23, R31, R33, R35, and R37 (0402 package) must not be populated (DNP).

2.4.1.3.3 FX-LOS Fiber Mode Strap

FX-LOS strap details are shown in Table 2-8. These strap settings determine if the ports are to operate in FX-LOS Fiber Mode or FX-SD/Copper Mode.

TABLE 2-8: FX-LOS MODE STRAP SETTINGS

R77 (10K)	R79 (10K)	Reference Voltage (V)	Function
Populate	DNP	3.3	A level above 2V selects FX-LOS for Port 0 and Port 1
Populate	Populate	1.5	A level of 1.5V selects FX-LOS for Port 0 and FX-SD / copper twisted pair for Port 1, further determined by FXSDB
DNP	Populate	0 (Default)	A level of 0V selects FX-SD / copper twisted pair for Ports 0 and 1, further determined by FXSDA and FXSDB

Note: The above strap details describe the LAN9252 function. This EVB does not support SFF Fiber Mode. Therefore, FX-SD related straps are not applicable.

2.4.2 LED Indicators

The D3 and D4 LEDs are used to indicate the Link/Activity status on the corresponding EVB ports, as detailed in Table 2-9. The Link/Act LED should be ON at each port when the cable is present. If the Link/Act LED is not ON, it indicates there is an issue with the connection or cable.

TABLE 2-9: D3 AND D4 LINK/ACTIVITY LED STATUS INDICATORS

State	Description
Off	Link is down
Flashing Green	Link is up with activity
Steady Green	Link is up with no activity

Additionally, the D5 LED is used as a RUN indicator (green) to shows the AL status of the EtherCAT® State Machine (ESM), as detailed in Table 2-10.

TABLE 2-10: D5 RUN LED STATUS INDICATOR

State	Description
Off	The device is in the INITIALIZATION state
Blinking (on 200ms, off 200ms)	The device is in the PRE-OPERATIONAL state
Single Flash (on 200ms, off 1000ms)	The device is in the SAFE-OPERATIONAL state
On	The device is in the OPERATIONAL state
Flickering (on 50ms, off 50ms)	The device is booting and has not yet entered the INITIALIZATION state, or the device is in the BOOTSTRAP state and firmware download is in progress. (Optional. Off when not implemented.)

2.4.3 EEPROM Switch

The EVB-LAN9252-DIG-IO utilizes 0x50 (7-bit) I^2C slave addressing. The SW3 switch can be used to select the A0, A1, and A2 address bits, as shown in Figure 2-2 and Table 2-11. The eighth bit of the slave address determines if the master device wants to read or write to the EEPROM (24C512).

FIGURE 2-2: SLAVE ADDRESS ALLOCATION

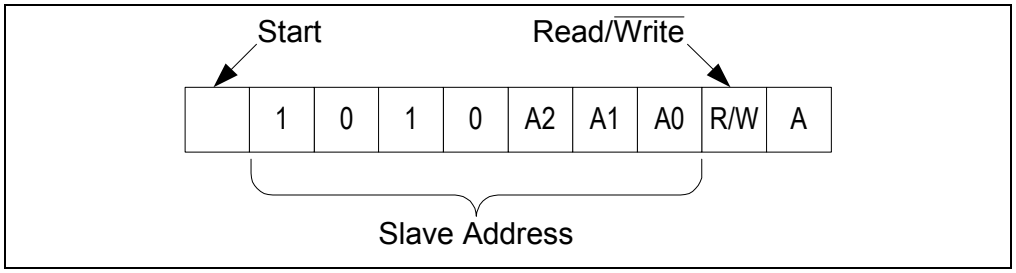


TABLE 2-11: EEPROM SWITCH

Switch	Description	Settings
SW3	I2C EEPROM address selection switch (A0, A1, A2). See Figure 2-2.	ON for logic 0 (default) OFF for logic 1

2.4.4 DIG INPUT Mode

The DIG INPUT Mode can be selected through the headers J10 and J11:

- Logic 1 : (Default) SW4 & SW5 Off position. DIG I/P 0 to 15 tied to pull-up (R98 to R113)
- Logic 0 : The respective knob of 2-way, 8-position dip switch (SW4 & SW5) need to be moved to ON side. Signals can be selected individually.

TABLE 2-12: DIGITAL I/O INPUT MODE SELECTION

Header	Description	Short Pins
J10	Digital Input 0 to 7	1&2, 4&5, 7&8, 10&11, 13&14, 16&17, 19&20, 22&23
J11	Digital Input 8 to 15	1&2, 4&5, 7&8, 10&11, 13&14, 16&17, 19&20, 22&23

2.4.5 DIG OUTPUT Mode

The DIG OUTPUT Mode can be selected through the headers J10 and J11. The updated Digital I/O values can be seen on the LEDs (D6 to D21):

- Logic 1 : LED illuminated
- Logic 0 : LED not illuminated.

Note: LED (D6 to D21) anode connected to ASIC.

TABLE 2-13: DIGITAL I/O OUTPUT MODE SELECTION (DEFAULT MODE)

Header	Description	Short Pins
J10	Digital I/O 0 to 7	2&3, 5&6, 8&9, 11&12, 14&15, 17&18, 20&21, 23&24
J11	Digital I/O 8 to 15	2&3, 5&6, 8&9, 11&12, 14&15, 17&18, 20&21, 23&24

Note: The control signal OE_EXT should be connected high by shorting J12 pins 15 and 16.

2.4.6 DIG Bidirectional Mode

The DIG Bidirectional Mode can be selected by shorting the respective test point pins with the headers J10 and J11, as detailed in Table 2-14. The input and output signal states in this mode are the same as detailed in **Section 2.4.4 "DIG INPUT Mode"** and **Section 2.4.5 "DIG OUTPUT Mode"**.

TABLE 2-14: DIGITAL I/O BIDIRECTIONAL MODE DESCRIPTION

Description	Short Pins
Digital I/O 0 to 7	TP5 & J10.1, TP6 & J10.4, TP7 & J10.7, TP8 & J10.10 TP9 & J10.13, TP10 & J10.16, TP11 & J10.19, TP12 & J10.22, TP13&J10.3, TP14&J10.6, TP15&J10.9, TP16& J10.12, TP17&J10.15, TP18&J10.18, TP19& J10.21, TP20&J10.24
Digital I/O 8 to 15	TP21 & J11.1, TP22 & J11.4, TP23 & J11.7, TP24 & J11.10, TP25 & J11.13, TP26 & J11.16, TP27 & J11.19, TP28 & J11.22, TP29&J11.3, TP30&J11.6, TP31&J11.9, TP32& J11.12, TP33&J11.15, TP34&J11.18,TP35& J11.21, TP36&J11.24

2.4.7 Control Signals

All control signals can be probed and controlled via the J12 header, as shown in Table 2-15.

TABLE 2-15: J12 HEADER CONTROL SIGNAL MAPPING

J12 Pin Number	J12 Signal	J12 Pin Number	J12 Signal
1	3V3	2	3V3
3	WD_STATE	4	GND
5	EOF	6	GND
7	SOF	8	GND
9	LATCH0	10	GND
11	LATCH1	12	GND
13	WD_TRIG	14	GND
15	OE_EXIT	16	3V3
17	OUTVALID	18	GND
19	LATCH_IN	20	GND

Note: J12 pins 15 & 16 must be shorted in output mode.

2.4.7.1 WD_STATE

This pin is the SyncManager Watchdog State output. A "0" indicates the watchdog has expired. The state of this signal can be seen in the LED D22.

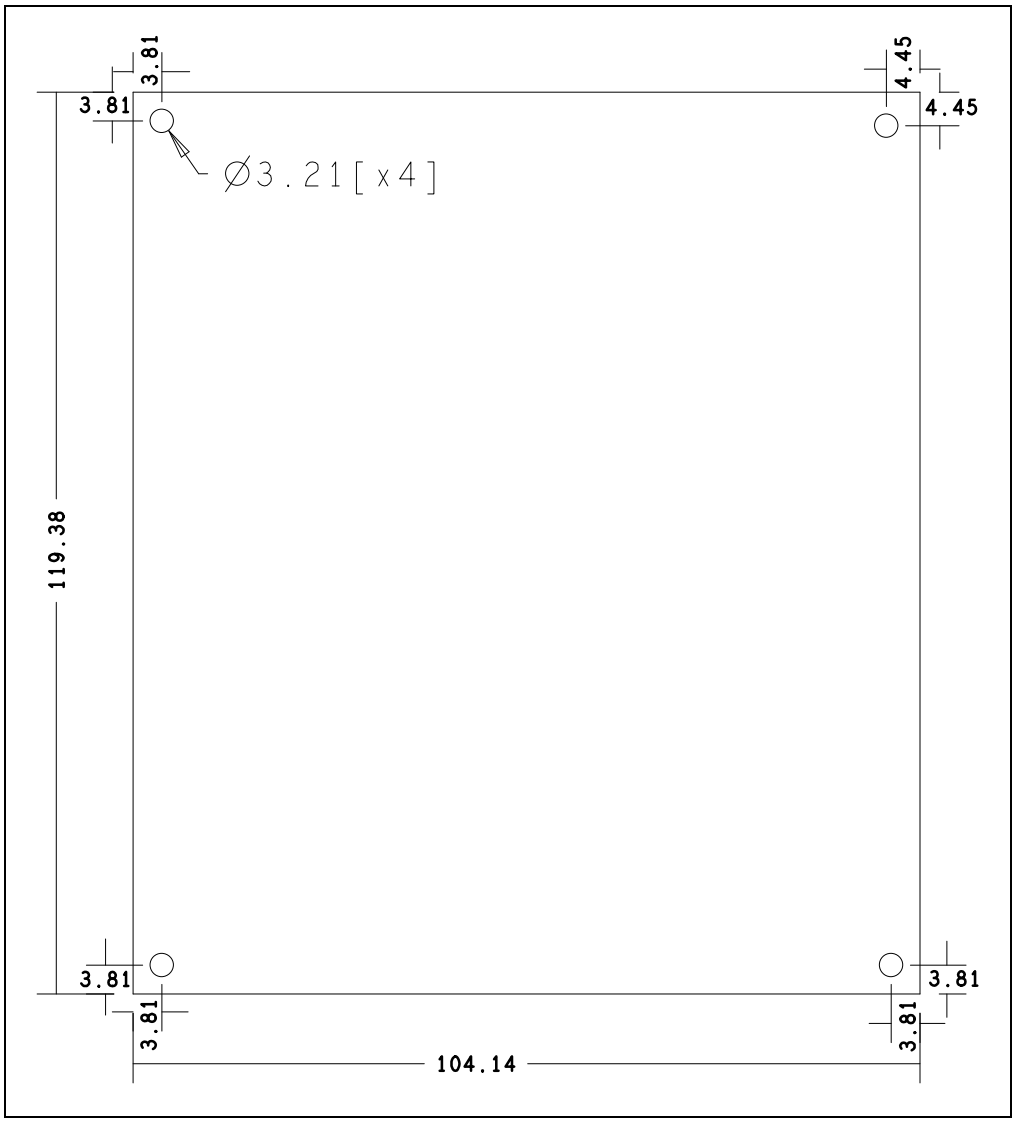
Note: This signal is not driven (high impedance) until the EEPROM is loaded.

2.4.7.2 LATCH_IN

This pin is the external data latch signal. The input data is sampled each time a rising edge of LATCH_IN is recognized. By default, this signals is pulled high through R131and can be made low using switch SW6.

2.5 MECHANICALS

FIGURE 2-3: EVB-LAN9252-DIG-IO MECHANICAL DIMENSIONS



Chapter 3. LAN9252 EEPROM Programming

3.1 PROGRAMMING THE LAN9252 EEPROM

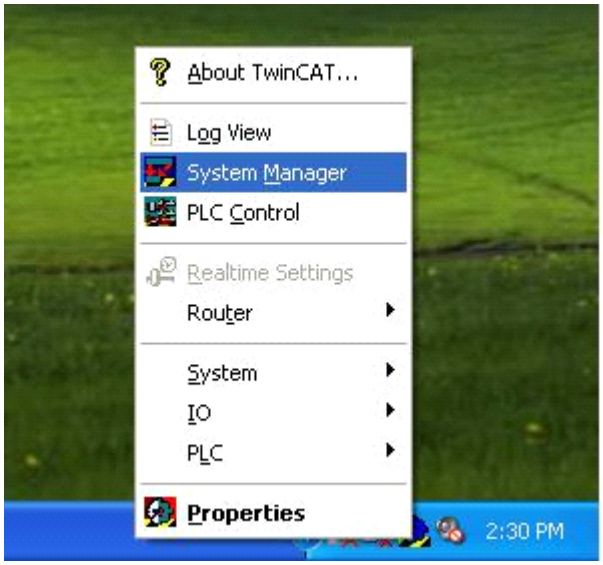
The LAN9252 configures itself to the desired mode (SPI, 6 HBI modes) by reading the strap settings located in EEPROM. The LAN9252 EEPROM is programmed and validated via the TwinCAT master tool. The programming procedure is as follows:

Note 1: This example utilizes the TwinCAT tool. Procedures may differ when using other EtherCAT® master tools.

2: Ensure the system network properties are configured properly for the EtherCAT® frames, Ethernet cable linking your system, and EtherCAT® slave board.

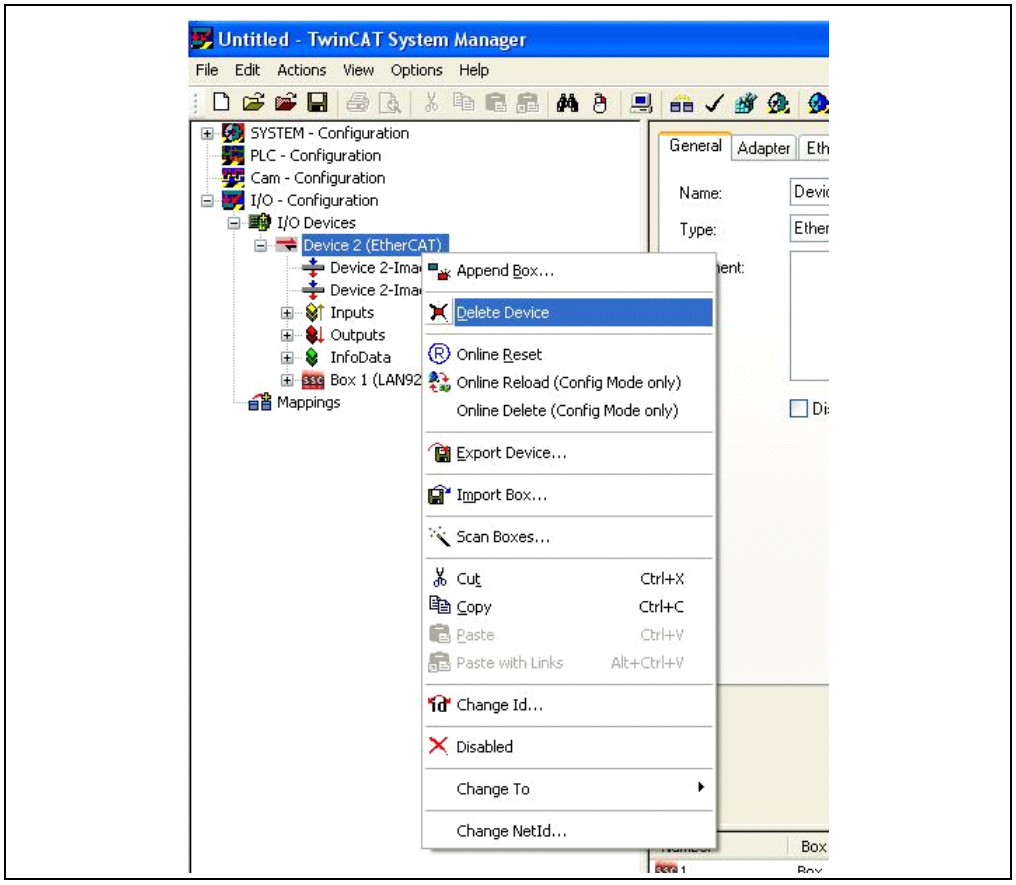
1. Load the corresponding ESI file in the directory path "C:\TwinCAT\Io\EtherCAT". For this demo, the ESI file for the 16-Bit Multiplexed Single-Phase Mode is used.
2. If TwinCAT installed successfully, a TwinCAT icon will be shown in the bottom-right corner of the desktop. After clicking the icon, a pop-up list will display. Select "System Manager", as shown in Figure 3-1.

FIGURE 3-1: TWINCAT SYSTEM MANAGER



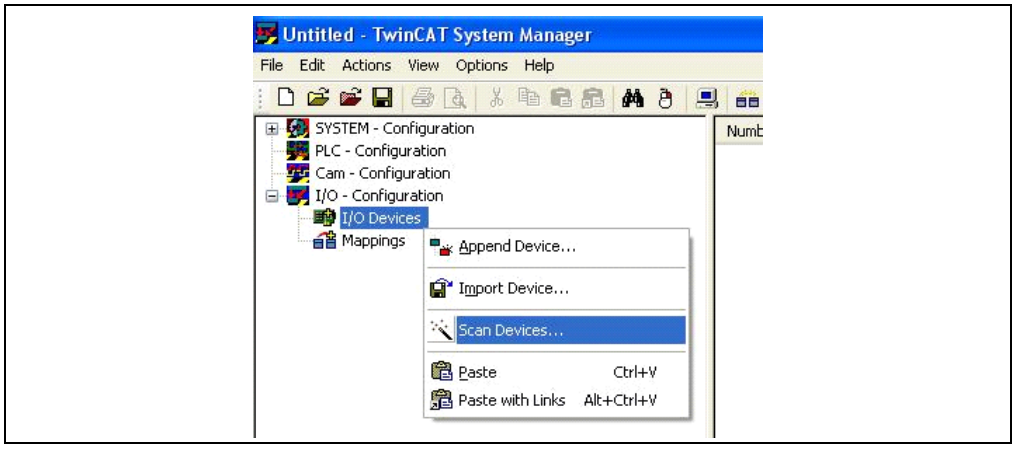
3. If any devices are present, delete them accordingly by clicking the device and selecting "Delete Device", as shown in Figure 3-2.

FIGURE 3-2: TWINCAT DELETE DEVICE



4. Scan for EtherCAT® slave devices by clicking "I/O devices" and selecting "Scan Devices", as shown in Figure 3-3.

FIGURE 3-3: TWINCAT SCAN DEVICES

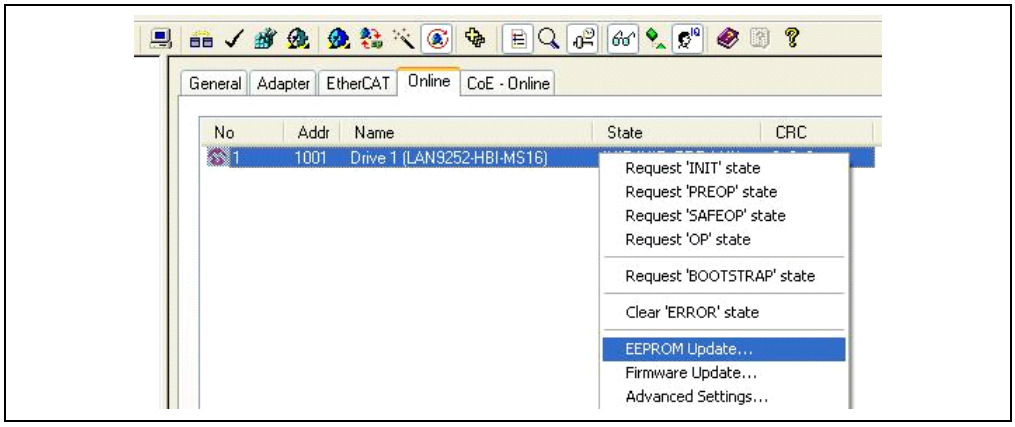


5. After scanning is complete, the right panel of the TwinCAT window will appear as shown in Figure 3-4.

FIGURE 3-4: TWINCAT DEVICE LIST

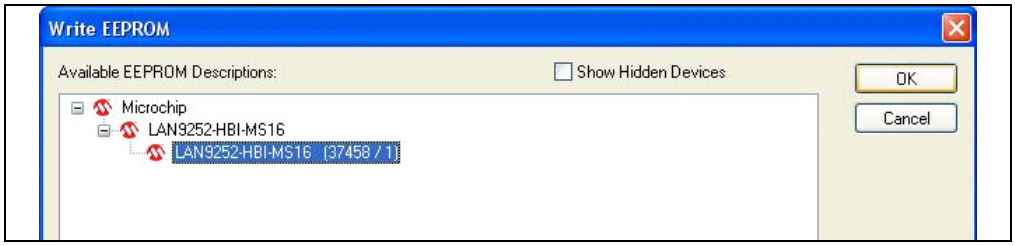
6. After a successful scan, click the “Device 2 (EtherCAT)” drop down bar on the left panel of the TwinCAT tool (as highlighted in Figure 3-4). Then click the “Online” tab on the right-side panel of the TwinCAT tool, as shown in Figure 3-5. Right click the LAN9252 listing and select “EEPROM Update” from the contextual menu.

FIGURE 3-5: TWINCAT EEPROM UPDATE



7. Upon selecting “EEPROM Update”, the Write EEPROM window will open. Click the “OK” button to initiate EEPROM programming.

FIGURE 3-6: TWINCAT WRITE EEPROM

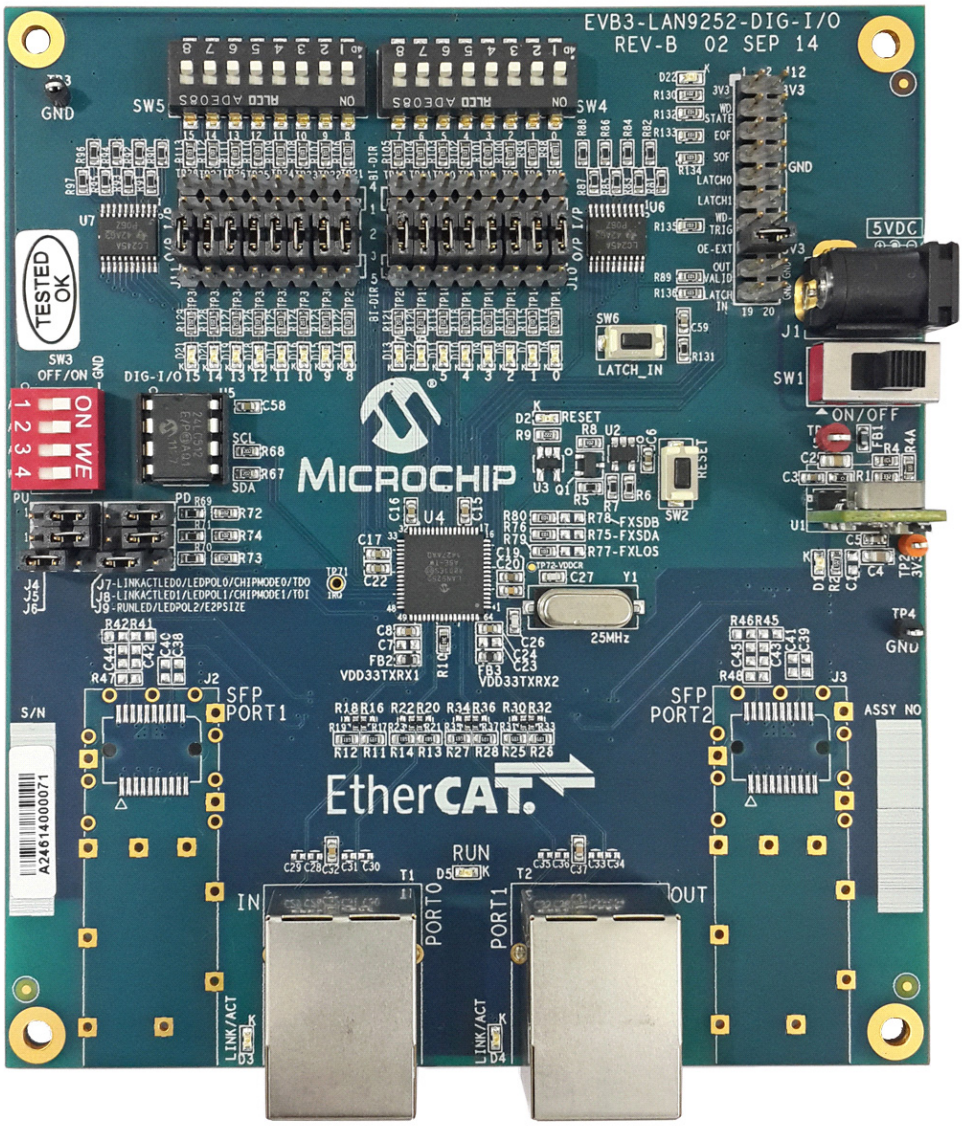


Appendix A. EVB-LAN9252-DIG-IO Evaluation Board

A.1 INTRODUCTION

This appendix shows the EVB-LAN9252-DIG-IO Evaluation Board.

FIGURE A-1: EVB-LAN9252-DIG-IO EVALUATION BOARD



Appendix B. EVB-LAN9252-DIG-IO Evaluation Board Schematics

B.1 INTRODUCTION

This appendix shows the EVB-LAN9252-DIG-IO Evaluation Board Schematics.

FIGURE B-1: EVB-LAN9252-DIG-IO SCHEMATIC POWER SUPPLY & RESET

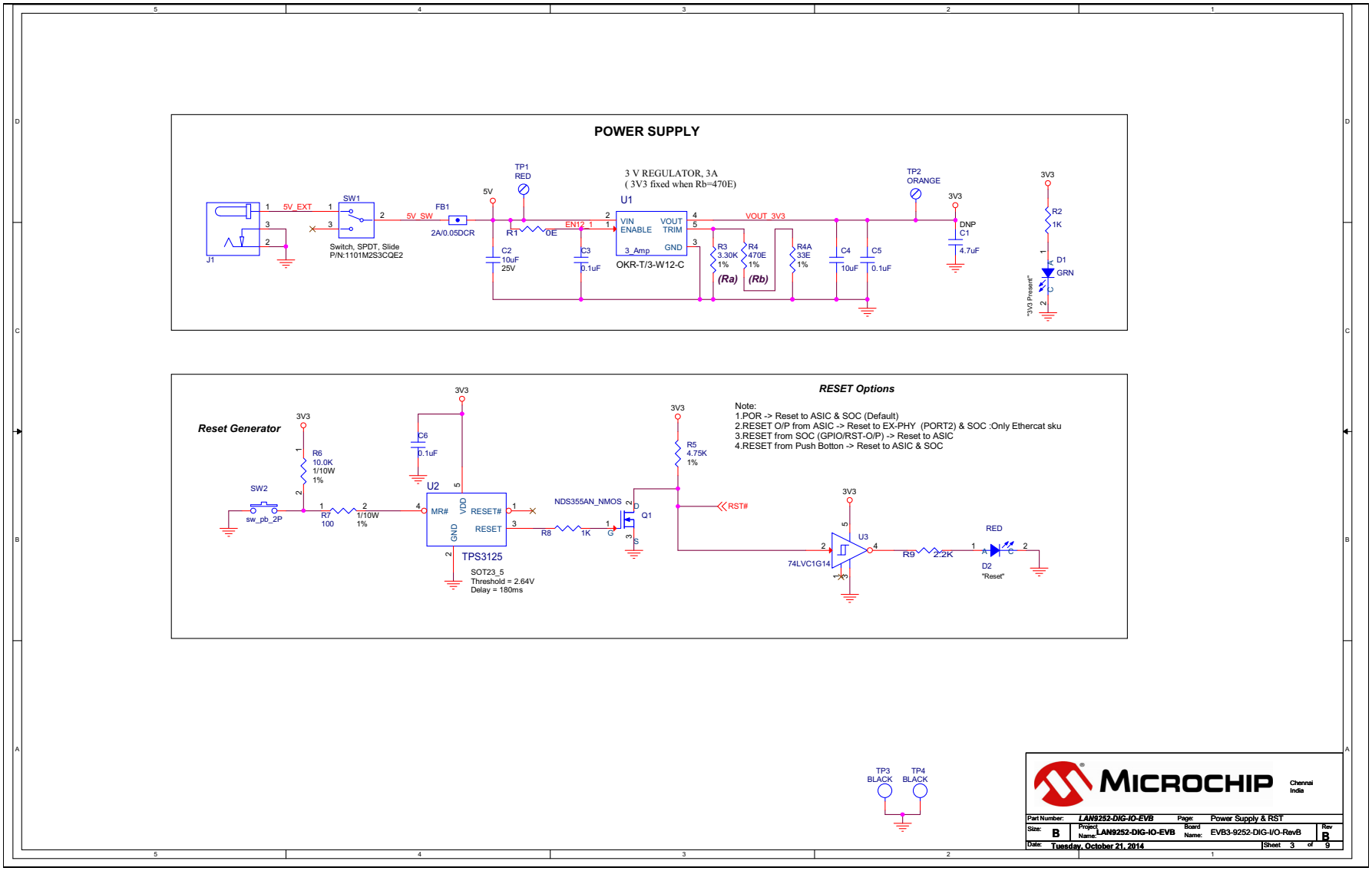


FIGURE B-2: EVB-LAN9252-DIG-IO SCHEMATIC LAN9252 PT1

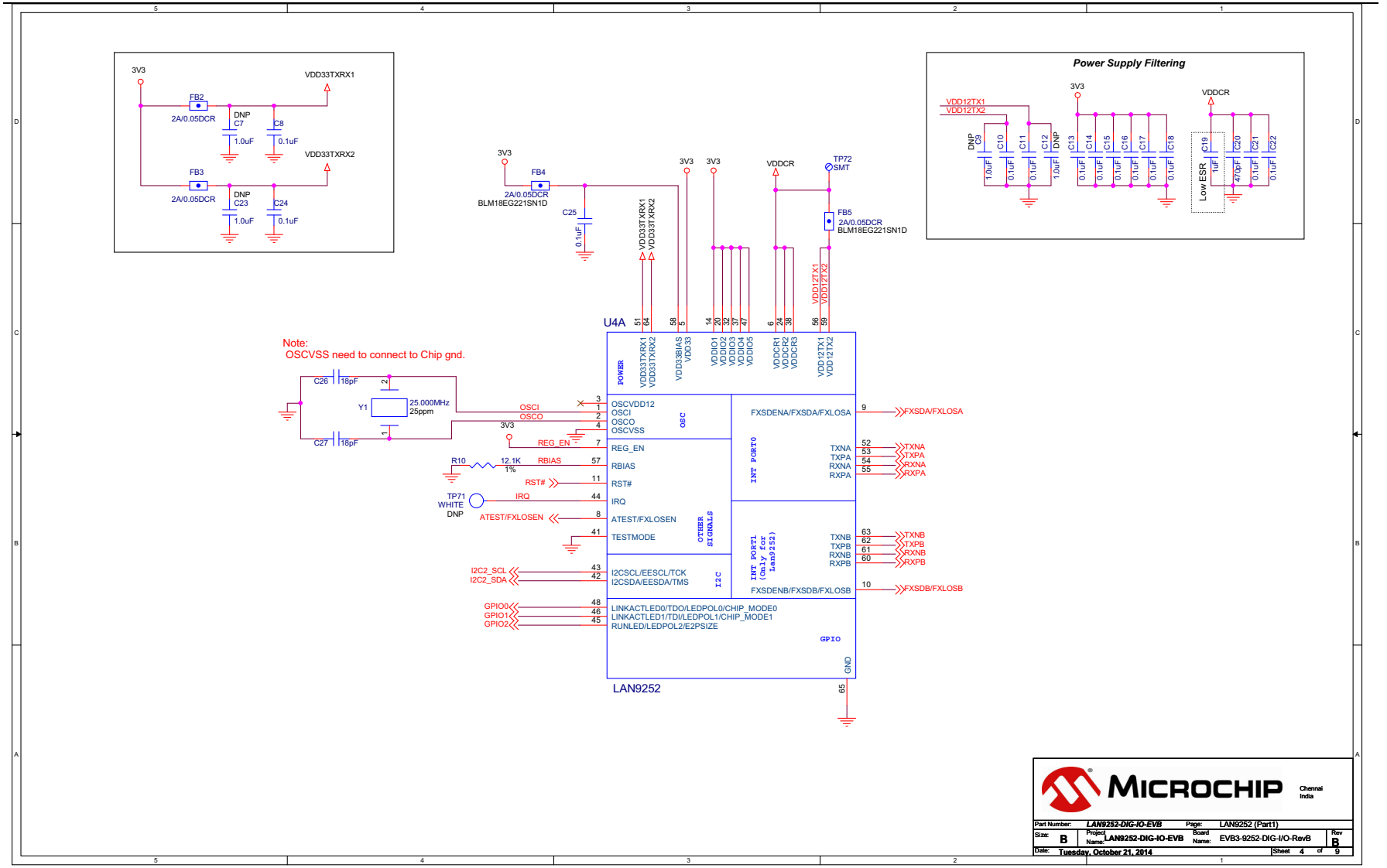


FIGURE B-3: EVB-LAN9252-DIG-IO SCHEMATIC COPPER MODE INTERFACE

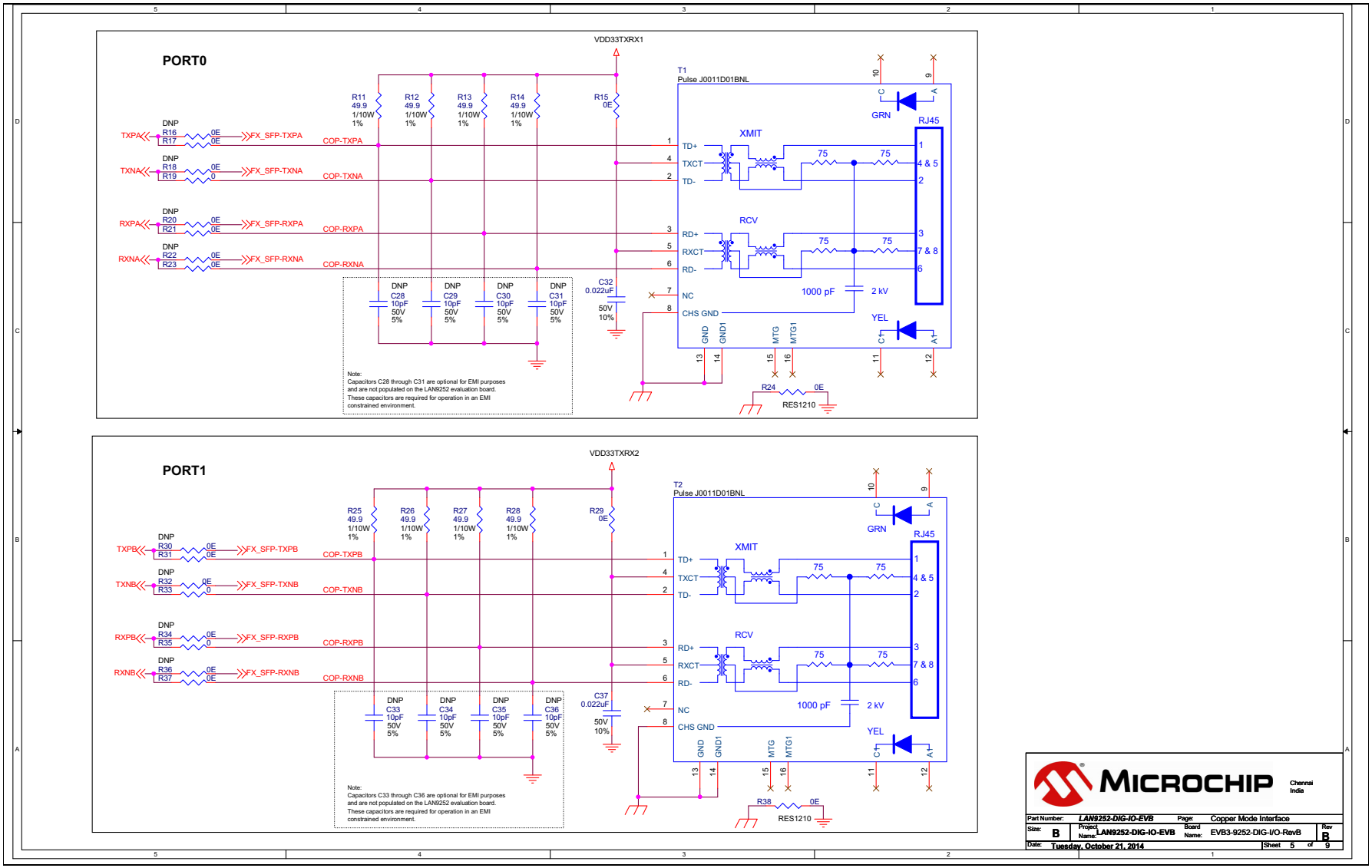


FIGURE B-4: EVB-LAN9252-DIG-IO SCHEMATIC SFP INTERFACE

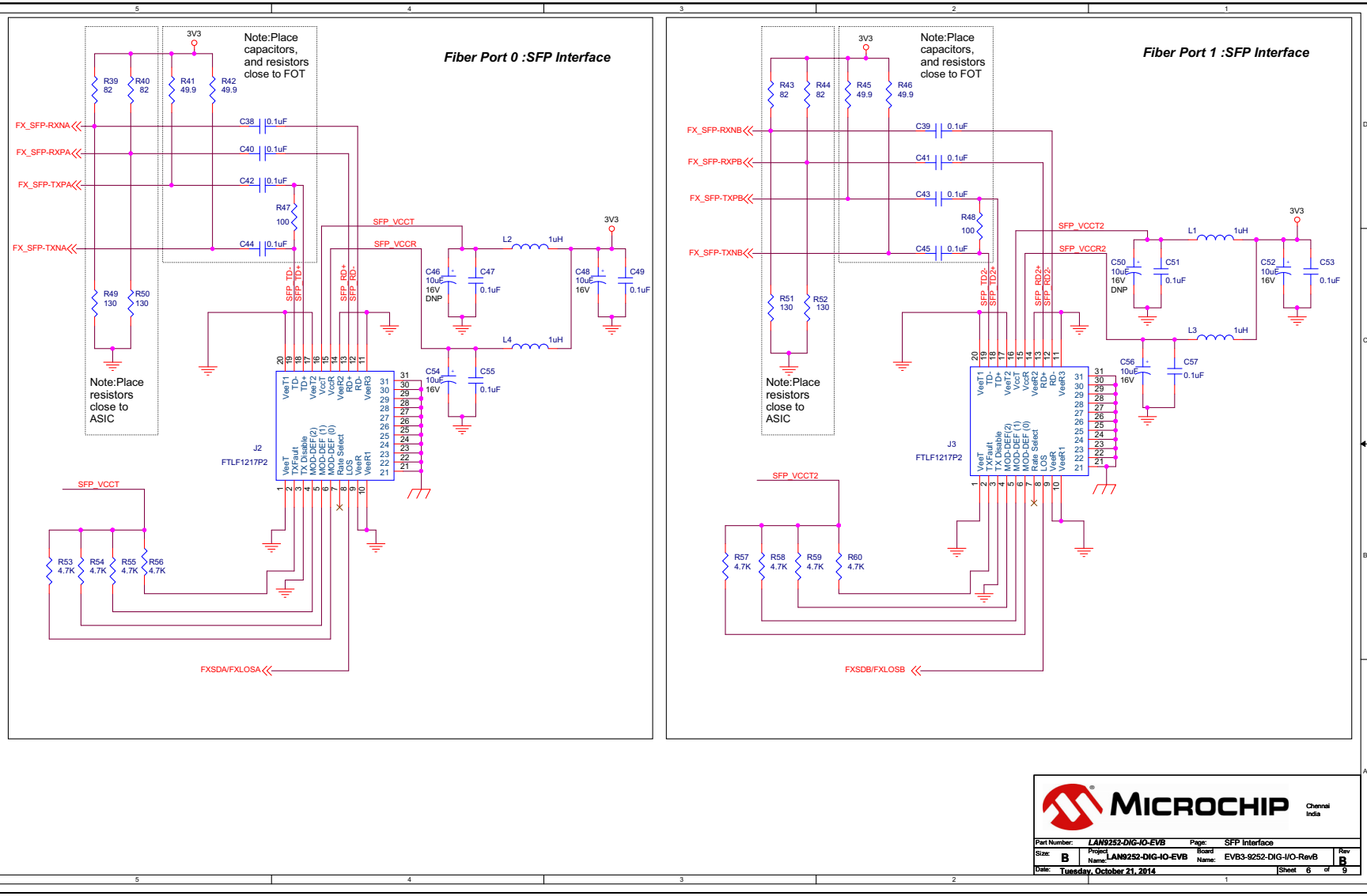
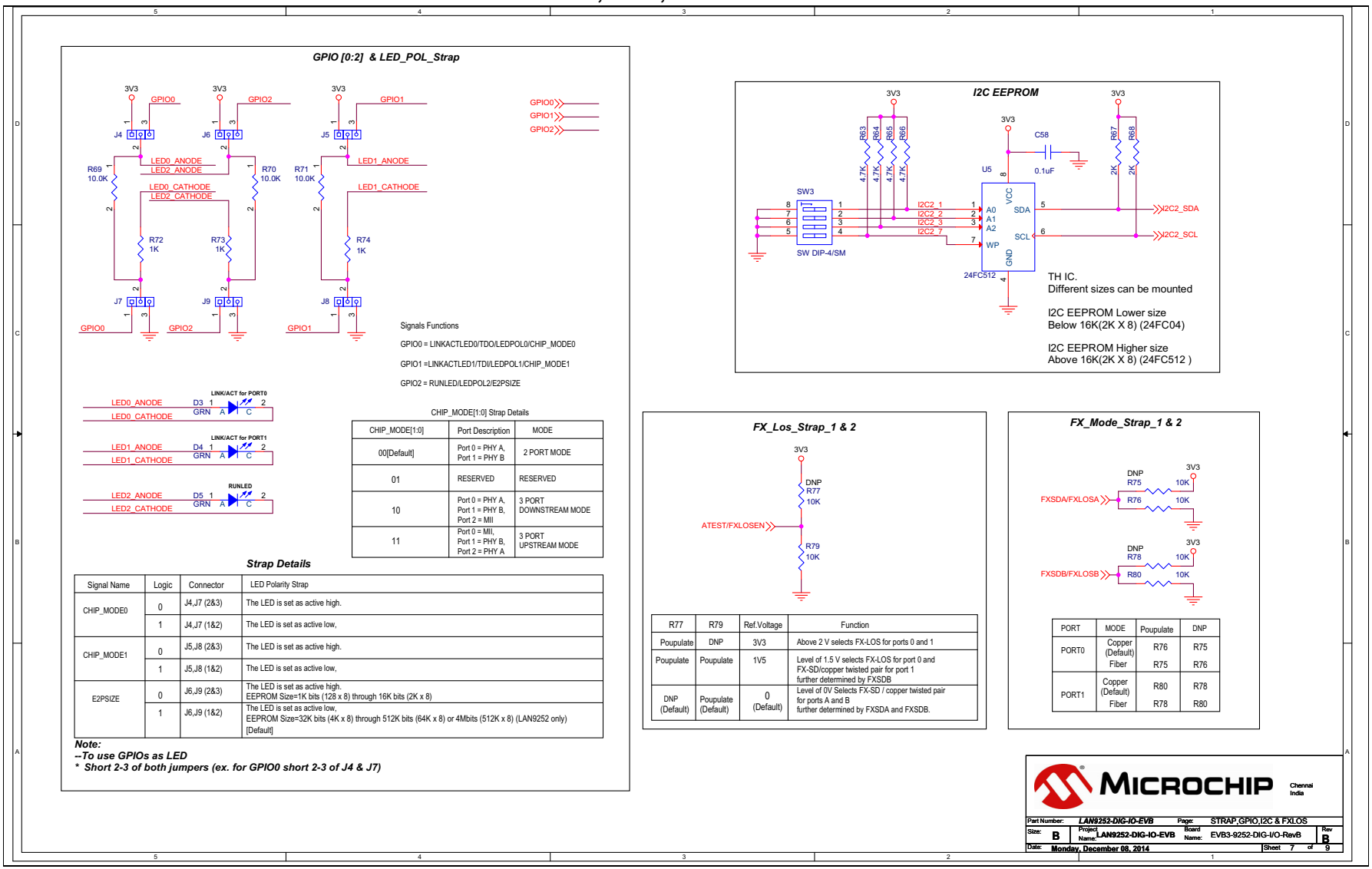


FIGURE B-5: EVB-LAN9252-DIG-IO SCHEMATIC STRAP, GPIO, I2C & FXLOS



CHIP_MODE[1:0]	Port Description	MODE
00[Default]	Port 0 = PHY A, Port 1 = PHY B	2 PORT MODE
01	RESERVED	RESERVED
10	Port 0 = PHY A, Port 1 = PHY B, Port 2 = MII	3 PORT DOWNSTREAM MODE
11	Port 0 = MII, Port 1 = PHY B, Port 2 = PHY A	3 PORT UPSTREAM MODE

Signal Name	Logic	Connector	LED Polarity Strap
CHIP_MODE0	0	J4,J7 (2&3)	The LED is set as active high.
	1	J4,J7 (1&2)	The LED is set as active low,
CHIP_MODE1	0	J5,J8 (2&3)	The LED is set as active high.
	1	J5,J8 (1&2)	The LED is set as active low,
E2PSIZE	0	J6,J9 (2&3)	The LED is set as active high. EEPROM Size=1K bits (128 x 8) through 16K bits (2K x 8)
	1	J6,J9 (1&2)	The LED is set as active low, EEPROM Size=32K bits (4K x 8) through 512K bits (64K x 8) or 4Mbits (512K x 8) (LAN9252 only) [Default]

R77	R79	Ref.Voltage	Function
Poupulate	DNP	3V3	Above 2 V selects FX-LOS for ports 0 and 1
Poupulate	Poupulate	1V5	Level of 1.5 V selects FX-LOS for port 0 and FX-SD/copper twisted pair for port 1 further determined by FXSDB
DNP (Default)	Poupulate (Default)	0 (Default)	Level of 0V Selects FX-SD / copper twisted pair for ports A and B further determined by FXSDA and FXSDB.

PORT	MODE	Poupulate	DNP
PORT0	Copper (Default)	R76	R75
	Fiber	R75	R76
PORT1	Copper (Default)	R80	R78
	Fiber	R78	R80

FIGURE B-6: EVB-LAN9252-DIG-IO SCHEMATIC LAN9252 PT2

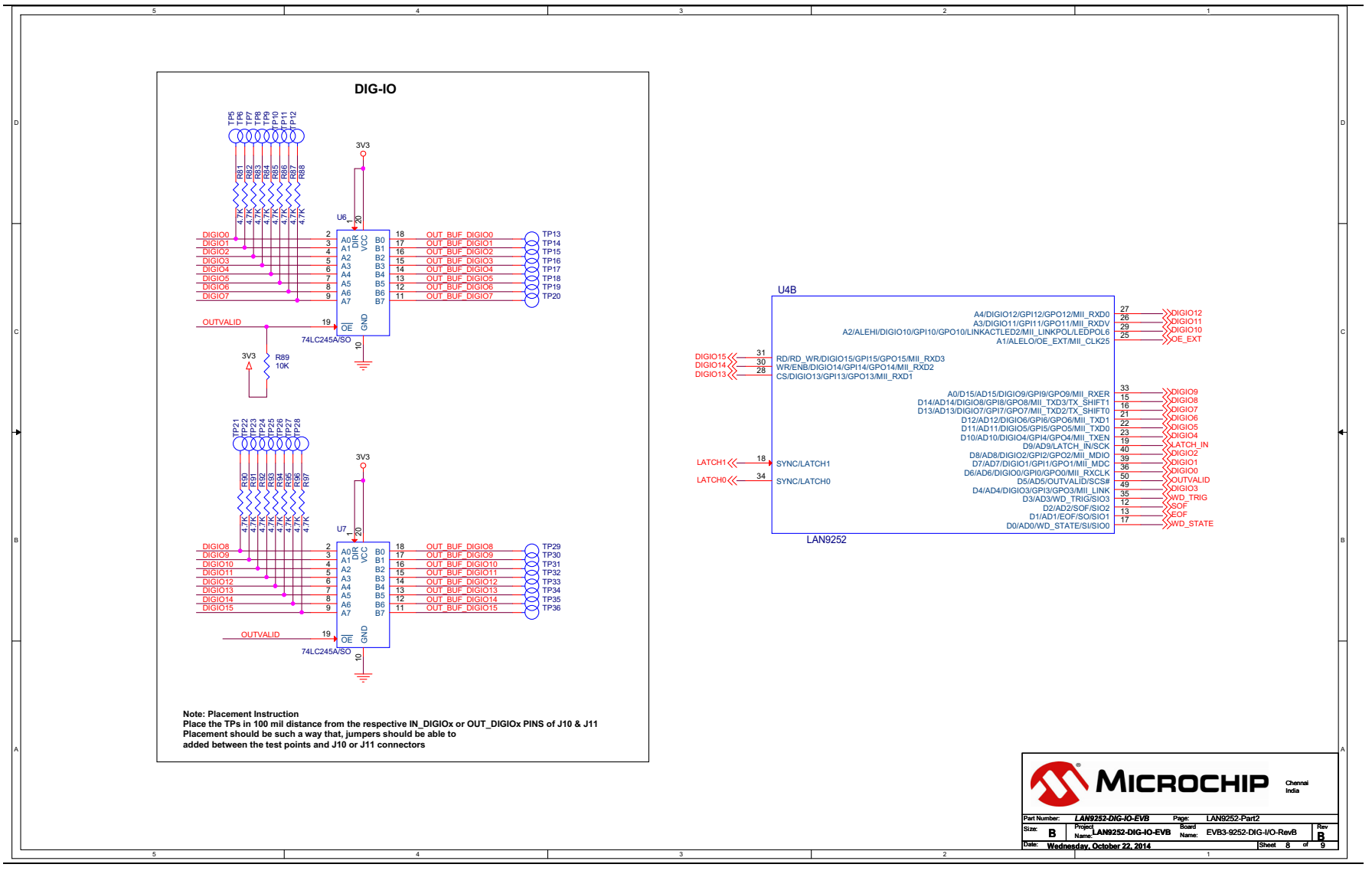
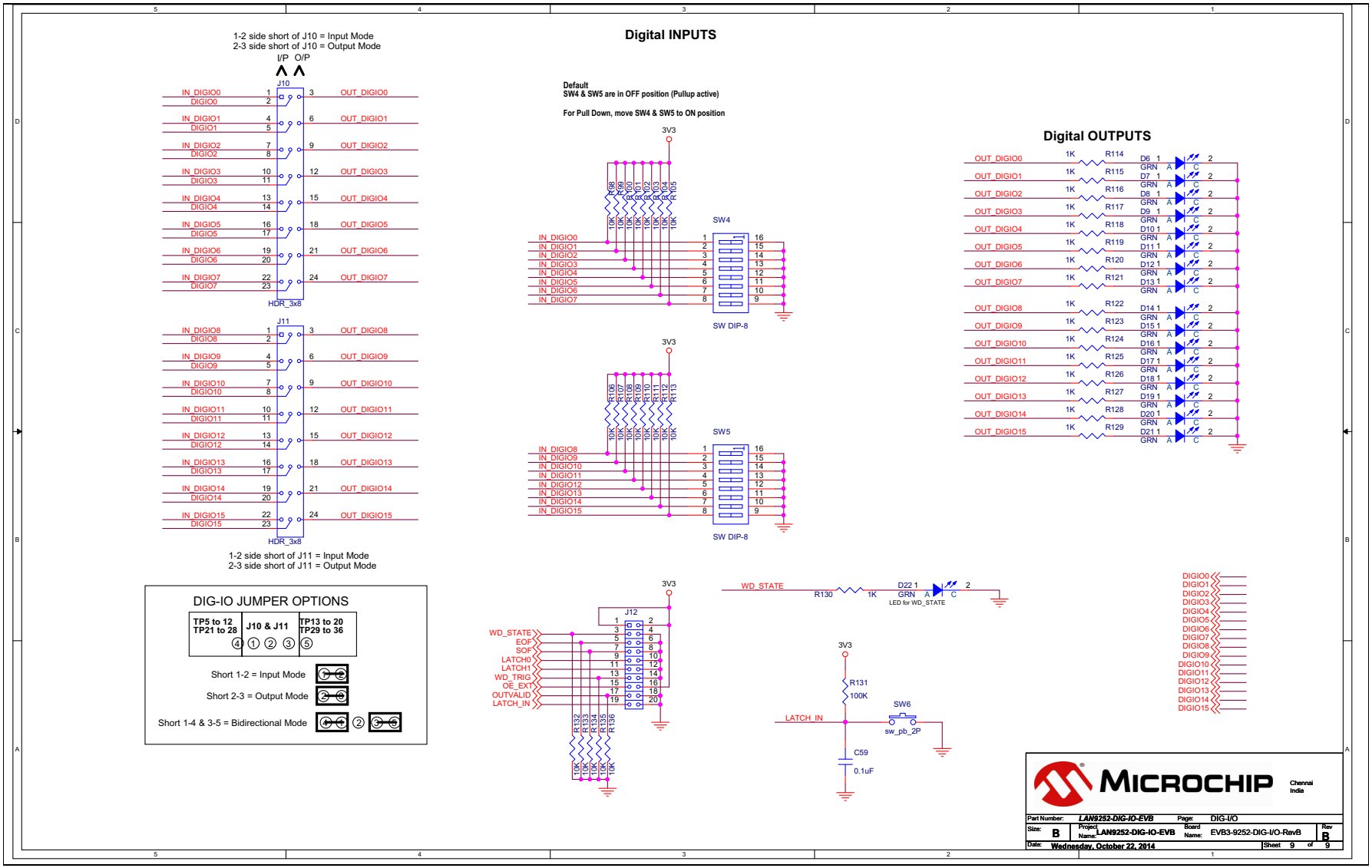


FIGURE B-7: EVB-LAN9252-DIG-IO SCHEMATIC DIGITAL I/O



Appendix C. Bill of Materials (BOM)

C.1 INTRODUCTION

This appendix includes the EVB-LAN9252-DIG-IO Evaluation Board Bill of Materials (BOM).

Item	Quantity	Reference	Part	PCB Footprint	DNP	Vender	Vender Part NO
1	2	C2,C4	10uF	CAP0805	No	Murata	GRM21BR61E106KA73L
2	18	C3,C5,C6,C8,C10,C11,C13,C14,C15,C16,C17,C18,C21, C22,C24,C25,C58,C59	0.1uF	CAP0603	No	Murata	GRM188R71E104KA01D
3	1	C19	1uF	CAP0603	No	Murata	GRM188R61C105KA93D
4	1	C20	470pF	CAP0603	No	Kemet	C0603C471K3RACTU
5	2	C26,C27	18pF	CAP0603	No	Murata	GRM1885C1H180JA01D
6	2	C32,C37	0.022uF	CAP0603	No	Kemet	C0603C223K5RACTU
7	21	D1,D3,D4,D5,D6,D7,D8,D9,D10,D11,D12,D13,D14,D15,D16,D17,D18,D19,D20,D21,D22	GRN	LED0603	No	Wurth electronics	150 060 GS7 500 0
8	1	D2	RED	LED0603	No	Wurth electronics	150 060 RS7 500 0
9	5	FB1,FB2,FB3,FB4,FB5	2A/0.05DCR	RES0603	No	Murata	BLM18EG221SN1D
10	1	J1	SKT_PWR_2R0mm_4A_THRU_RA	th_conn_pwrjack_dc-210_rt	No	Cui Stack	PJ-002AH
11	6	J4,J5,J6,J7,J8,J9	HDR_1x3	TH_CONN_1X3P	No	FCI	68000-103HLF
12	2	J10,J11	HDR_3x8	TH_CONN_3x8P	No	FCI	68000-108HLF
13	1	J12	2x10	TH_CONN_2x10P	No	FCI	67997-220HLF
14	1	Q1	NDS355AN_NMOS	sot23-NDS	No	Fairchild	NDS355AN
15	3	R1,R15,R29	0E	RES0603	No	Panasonic	ERJ-3GEY0R00V
16	22	R2,R8,R72,R73,R74,R114,R115,R116,R117,R118,R119,R120,R121,R122,R123,R124,R125,R126, R127,R128,R129,R130	1K	RES0603	No	Panasonic	ERJ-3GEYJ102V
17	1	R3	3.30K	RES0603	No	Yageo America	9C06031A3301FKHFT
18	1	R4	470E	RES0603	No	BOURNS	CR0603-FX-4700ELF
19	1	R4A	33E	RES0603	No	BOURNS	CR0603-FX-33R0ELF
20	1	R5	4.75K	RES0603	No	Panasonic	ERJ-3EKF4751V
21	4	R6,R69,R70,R71	10.0K	RES0603	No	Panasonic	ERJ-3EKF1002V
22	1	R7	100	RES0603	No	Panasonic	ERJ-3EKF1000V
23	1	R9	2.2K	RES0603	No	Panasonic	ERJ-3GEYJ222V
24	1	R10	12.1K	RES0603	No	Rohm	MCR01MZPF1202
25	8	R11,R12,R13,R14,R25,R26,R27,R28	49.9	RES0603	No	Yageo America	9C06031A49R9FKHFT
26	8	R17,R19,R21,R23,R31,R33,R35,R37	0E	RES0402	No	Panasonic	ERJ-2GE0R00X

27	2	R24,R38	0E	RES1210	No	Vishay	CRCW12100000Z0EA
28	2	R67,R68	2K	RES0603	No	Panasonic	ERJ-3GEYJ202V
29	25	R76,R79,R80,R89,R98,R99,R100,R101,R102,R103,R104,R105,R106,R107,R108,R109,R110,R111,R112,R113,R132,R133,R134,R135,R136	10K	RES0603	No	Panasonic	ERJ-3GEYJ103V
30	1	R131	100K	RES0603	No	Panasonic	ERJ-3EKF1003V
31	20	R81,R82,R83,R84,R85,R86,R87,R88,R90,R91,R92,R93,R94,R95,R96,R97,R63,R64,R65,R66	4.7K	RES0603	No	Panasonic	ERJ-3EKF4701V
32	1	SW1	SW-SPDT-SLIDE	sw_ck_1101m2s3cqe2	No	C&K	1101M2S3CQE2
33	2	SW2,SW6	sw_pb_2P	sw_pb_2P	No	Panasonic	EVQ-PJU04K
34	1	SW3	SW DIP-4/SM	TH_SW_DIP4	No	Wurth electronics	418117270904
35	2	SW4,SW5	SW DIP-8	SW_DIP_SMT_8P-ade08s04	No	TE	1-1825058-9/ade08s04
36	1	TP1	RED	TH_TP_60D40	No	Keystone	5000
37	1	TP2	ORANGE	TH_TP_60D40	No	Keystone	5003
38	2	TP3,TP4	BLACK	TH_TP_60D40	No	Keystone	5001
39	32	TP5,TP6,TP7,TP8,TP9,TP10,TP11,TP12,TP13,TP14,TP15,TP16,TP17,TP18,TP19,TP20,TP21,TP22,TP23,TP24,TP25,TP26,TP27,TP28,TP29,TP30,	WHITE	TH_TP	No	FCI	68000-101HLF
40	2	T1,T2	Pulse - J0011D01BNL	th_conn_pulse_rj45_j0026	No	Pulse Electronics	J0011D01BNL
41	1	U1	3_Amp	TH_DC-DC_VERT_5PIN_P67	No	Murata	OKR-T/3-W12-C
42	1	U2	TPS3125	SOT23_5	No	TI	TPS3125L30DBVR
43	1	U3	74LVC1G14	SOT23_5	No	TI	SN74L VCIG14DBVR
44	1	U4	LAN9252	IC_QFN64	No	Microchip	LAN9252
45	1	U5	24FC512	IC_DIP8_300	No	Microchip	24FC512-I/P
46	2	U6,U7	74LC245A/SO	IC_SO20-MO-153	No	TI	SN74LVC245APWR
47	1	Y1	25.000MHz	XTAL_HCM49	No	Cardinal Components Inc.	CSM1Z-A5B2C5-40-25.0D18-F

Do NOT Populate components:

Item	Quantity	Reference	Part	PCB Footprint	DNP	Vender	Vender Part NO
1	1	C1	4.7uF	CAP0603	DNP	Murata	GRM188R60J475KE19D
2	4	C7,C9,C12,C23	1.0uF	CAP0603	DNP	Murata	GRM188R61C105KA93D
3	8	C28,C29,C30,C31,C33,C34,C35,C36	10pF	CAP0402	DNP	Murata	GRM1885C1H100JA01D
4	14	C38,C39,C40,C41,C42,C43,C44,C45,C47,C49, C51,C53,C55,C57	0.1uF	CAP0603	DNP	Murata	GRM188R71E104KA01D
5	6	C46,C48,C50,C52,C54,C56	10uF	CAP_B_3528	DNP	Kemet	B45190E3106K209
6	2	J2,J3	FTLF1217P2	CONN_FX_SFP_FTLF1217P2	DNP	Finisar	775-1011-ND
7	4	L1,L2,L3,L4	1uH	L0805	DNP		
8	8	R16,R18,R20,R22,R30,R32,R34,R36	0	RES0402	DNP		
9	4	R39,R40,R43,R44	82	RES0603	DNP	Panasonic	ERJ-3EKF1300V
10	4	R41,R42,R45,R46	49.9	RES0603	DNP	Yageo America	9C06031A49R9FKHFT
11	2	R47,R48	100	RES0603	DNP	Panasonic	ERJ-3EKF1000V
12	4	R49,R50,R51,R52	130	RES0603	DNP	Panasonic	ERJ-3EKF1300V
13	8	R53,R54,R55,R56,R57,R58,R59,R60	4.7K	RES0603	DNP	Panasonic	ERJ-3EKF4701V
14	3	R75,R77,R78	10K	RES0603	DNP	Panasonic	ERJ-3GEYJ103V
15	1	TP71	WHITE	TH_TP_60D40	DNP	Keystone	5002
16	1	TP72	SMT	tp-smd40	DNP	NA	NA

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Fax: 33-1-69-30-90-79

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