



IQS680 Datasheet

Combination sensor with dual channel capacitive proximity/touch, Pyroelectric Infrared Radial sensor and metal detection capabilities

The IQS680 ProxFusion® IC is a multifunctional Capacitance, Pyroelectric Infrared Radial (PIR) & Inductance sensor designed for applications such as domestic energy efficient lighting applications with movement detection. The IQS680 is an ultra-low power solution designed for short or long term activations through any of the sensing channels. The IQS680 operates standalone or via the I²C protocol and custom configurations are stored in an on-chip EEPROM.

Features

- **Unique combination of Sensors:**
 - Capacitive Sensing
 - Inductive Sensing
 - PIR Sensing
- **Capacitive Sensing**
 - 2pF to 200pF external capacitive load capability
 - Fully adjustable sensing options
 - Mutual- or self-capacitance.
- **Inductive Sensing**
 - Distinguish between ferrous and non-ferrous metals
 - Only external sense coil required (PCB trace)
- **PIR Sensing:**
 - DSP algorithm for long range movement detection.
 - Automatic drift compensation.
- **Multiple integrated UI's**
- **Automatic Tuning Implementation (ATI)** – performance enhancement (10bit ATI)
- **EEPROM** included on-chip for calibration data and settings.
- Minimal external components
- Standard I²C interface (polling with sub 1ms clock stretching)
- Optional RDY indication for standalone mode

operation

- **Low Power Consumption:**
 - 300uA
 - (100 Hz response)
 - 10uA
 - (10 Hz response)
- **Supply Voltage:** 1.75V to 3.6V



DFN 3 x 3 x 0.7

10-Pin

Representations only, not actual markings

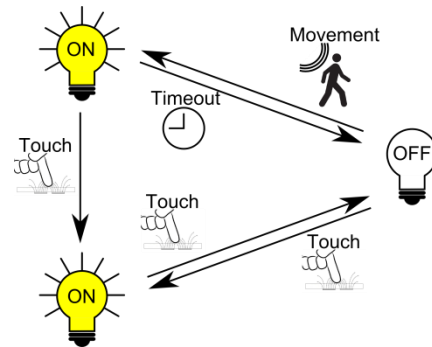


Figure 1: Under cabinet UI (PIR and Prox)

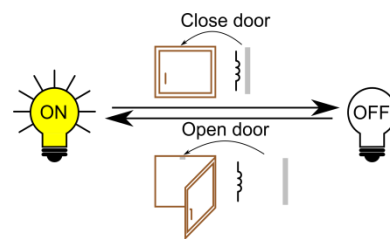


Figure 2: In cabinet UI (Inductive sensor)

Applications

- Under Cabinet Lighting (UCL)
- Standard PIR sensor cost reduction
- Smart Lights
- Night Lights
- Battery powered PIR sensors solutions
- Movement detection

Available Packages	
T_A	DFN10
-20°C to 85°C	IQS680



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List of Abbreviations

ATI	Automatic Tuning Implementation
BOD	Brown Out Detection
FOV	Field Of View
GND	Ground
I ² C	Inter-Integrated Circuit
ICI	Internal Capacitor Implementation
LTA	Long Term Average
MSL	Moisture Sensitivity Level
OTP	One-Time Programmable
PIR	Pyroelectric Infrared Radial
POR	Power On Reset
PWM	Pulse Width Modulation
THR	Threshold
TO	Time-Out
UI	User Interface

List of symbols

C _{ATI}	ATI Compensation
CS _{PIR}	PIR sensor Counts
CS _{SS}	Steady-State CS _{PIR}
CS _T	Touch Counts
C _S	Internal Reference Capacitor
C _X	Sense electrode
D _{THR}	PIR Counts Deviation Threshold
f _S	Sampling frequency
M _{ATI}	ATI Multiplier
P _{THR}	Proximity event Threshold
R _X	Receiving electrode
T _{THR}	Touch event Threshold
T _X	Transmission electrode
V _{DD}	Supply voltage
V _{SS}	Ground



1 Introduction

1.1 ProxFusion®

The ProxFusion® sensor series provide all the proven ProxSense® engine capabilities with additional sensors types. A combined sensor solution is available within a single platform.

1.2 Packaging and Pin-Out

The IQS680 is available in the DFN10 packaging. The pin-outs and functionality are given below.

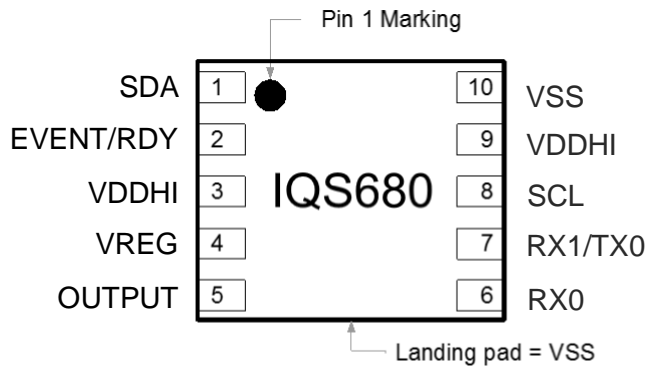


Figure 1.1: IQS680 pin-out (DFN10 package; device markings may differ)

Table 1-1: Pin-out descriptions

Pin	Name	Type	Function
1	SDA	I ² C	SDA (I ² C Data signal)
2	EVENT	Digital Out	Active output on movement and when PIR is blocked
2	RDY	I ² C	RDY (I ² C Ready interrupt signal)
3	VDDHI	Supply Input	Supply: 1.75V – 3.6V
4	VREG	Regulator output	Requires external capacitors
5	OUTPUT	Digital Out	Active high/low open-drain/push-pull output with PWM
6	Rx0	Analogue	Charge Receive electrode for sensors
7	Rx1	Analogue	Charge Receive electrode for sensors
7	Tx0	Analogue	Charge Transfer electrode for sensors
8	SCL	I ² C	SCL (I ² C Clock signal)
9	VDDHI	Supply Input	Supply: 1.75V – 3.6V
10	VSS	Voltage reference	Ground connection



1.3 Reference schematic

The PIR can be powered from either VREG or VDD. For long range (> 1m) applications, it is suggested to power the PIR from VDD. For shorter range and lower power applications it is suggested to power the PIR from VREG. An RC filter is placed at the PIR output if required. The PIR sensors need to be placed as close as possible to the IQS680 to ensure RF immunity. Bypass capacitors can be used on the output signal of the PIR as well as the power supply rails to remove unwanted noise. As seen in Figure 1-2, noise suppression components can be added if a problem is experienced with noise. These components can be changed based on the noise requirements of the application. Resistor **R5** and needs to be added if the PIR sensor can not be placed close to the IC. Resistors **R6**, **R7**, **R11** and **R13** is calculated based on the bias current requirement of the PIR element. If using the Inductive UI **R4** and **R5** should be replaced with a ferrite bead to increase RF immunity.

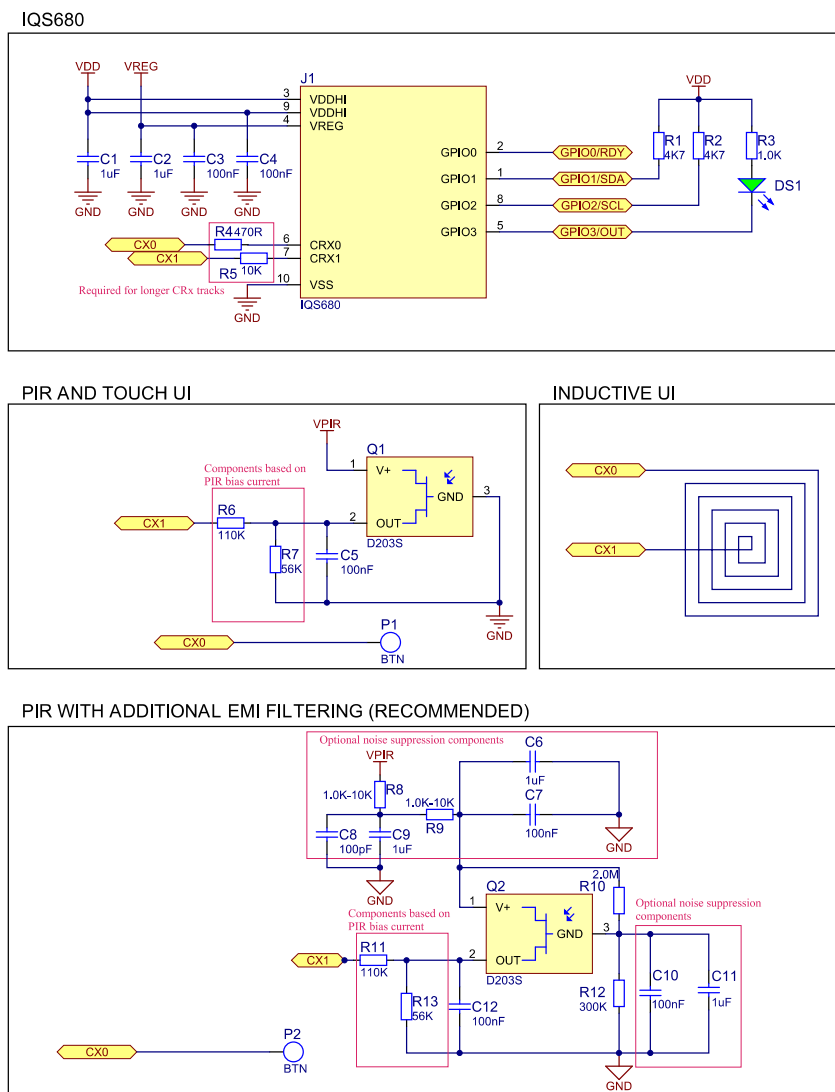


Figure 1.2 IQS680 reference schematic



1.4 Sensor channel combinations

The table below summarizes the IQS680's sensor and channel associations.

Table 1-2 Sensor - channel allocation

	Sensor / UI type	CH0	CH1	CH2
Capacitive	Movement detection	○ Touch	● PIR	
Inductive	Metal detection	○ Touch rejection		● Inductive

Key:

- - Optional implementation
- - Fixed use for UI

1.5 Features

The IQS680 is a capacitive sensing controller designed for both integrated and standalone Pyroelectric Infrared Radial (PIR) sensing applications. The device offers highly dynamic and adjustable PIR sensing range, depending on the lens chosen (0 – 10m), as well as a high sensitivity proximity (Prox) and contact (Touch) detection through a dedicated sensor line (C_x).

The device includes advanced Digital Signal Processing (DSP) capabilities for on-chip PIR signal analysis. This, combined with the Automatic Tuning Implementation (ATI) algorithm which calibrates the device to the sense electrode, yields a highly stable, high sensitivity movement detection controller. Further features of the device include an internal voltage regulator and Internal Capacitor Implementation (ICI) to reduce external components. The analogue circuitry is also capable of Power On Reset (POR) detection as well as Brown Out Detection (BOD).

Furthermore, the device has an inductive sensing mode that allows for the detection of non-ferret metals near the sensor.

The device can also be configured by means of an on-chip EEPROM, such as choosing the device output format, event durations, sensitivity and storing calibration data. The output options include an open-drain or push-pull, active high or low output with Pulse Width Modulation (PWM) as well as the standard I²C interface.

1.6 Operation

The device has been designed to be used in standalone battery operated automated lighting applications with on/off touch control capabilities. Furthermore, standard I²C interface allows the device to be used in an integrated environment.

The capacitive sensing line of the device can reliably observe the measured results at various levels, which enables it to distinguish between a Prox or Touch event. This allows for a variety of User Interface (UI) responses. The ATI algorithm allows for the adaptation to a wide range of sensing pad sizes.



2 User Interface

Although standard I²C interface is available, the IQS680 is designed as a standalone device with a single logic output. There are three User Interfaces (UI's) on the device, namely Movement detection, Touch detection and Metal detection. The first UI uses a PIR sensor to detect movement over a distance and the second senses touch by means of a capacitive sensing electrode (C_x). The latter

operates with a single copper coil to detect non-ferrite metals in close proximity.

Flow-diagrams of the three UI's are given in Figure 2.1 below. Note that when the output is in PWM mode, it is not considered to be in an active state. More detail is provided on this in the subsections that follow.

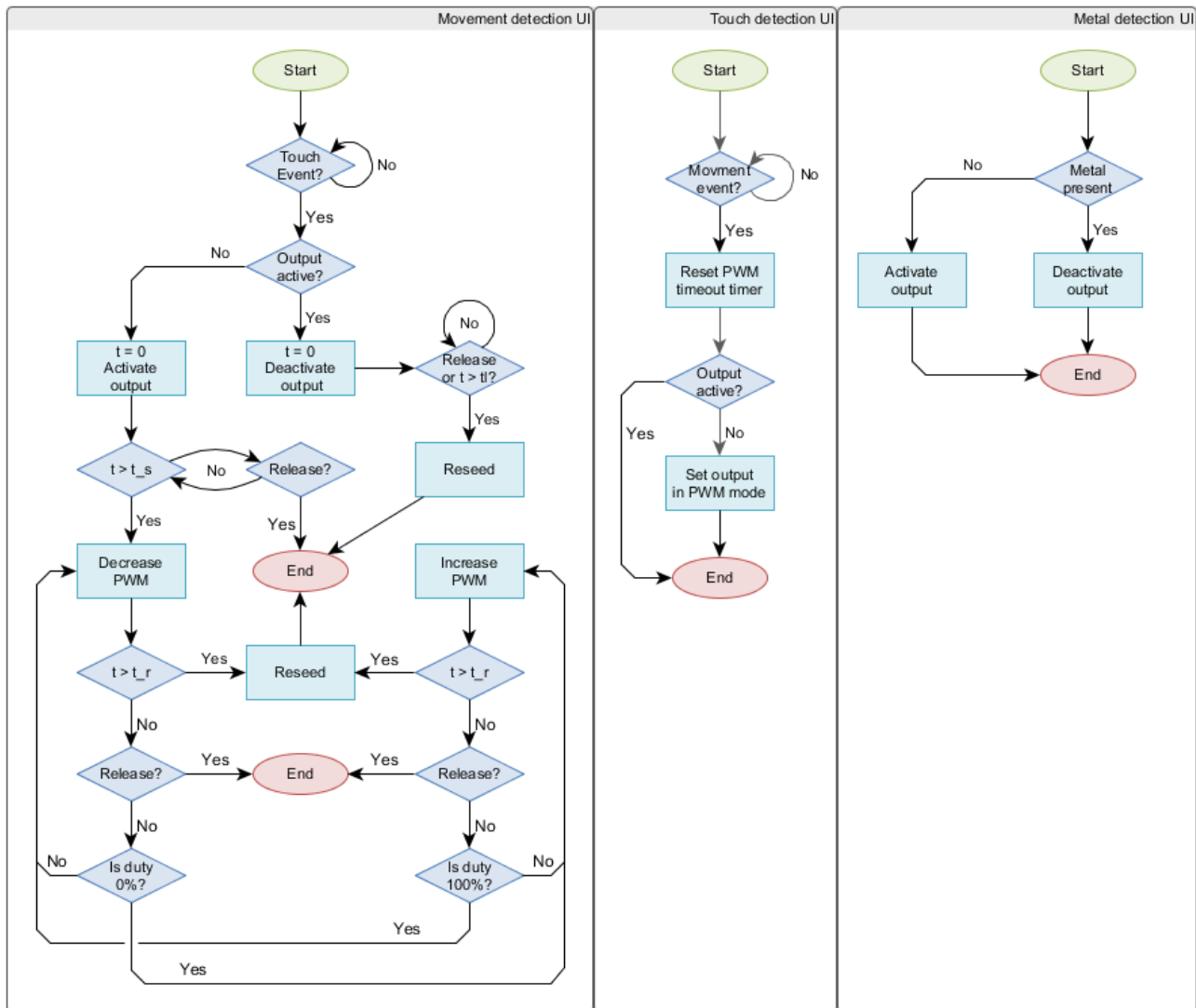


Figure 2.1: UI flow-diagrams



2.1 Movement detection UI

2.1.1 PIR sensor

The PIR sensor functions as the movement over a distance interface. Typical PIR sensors have a sensing range of up to 10m, with a radial FOV of 120°. Care should be taken when designing the housing of the PIR sensor as well as the choice of lens, as this plays a pivotal role in sensitivity, range and FOV of the PIR sensor.

Given that the output is in an inactivate state, the IQS680 will switch the output into PWM mode if any movement is detected within the PIR's FOV. The output will exit PWM mode after a predefined time period, upon which the output will return to an idle state.

However, if movement is detected whilst the output is already in PWM mode, the deactivation timers will be reset. This implies that the device will only return to an idle state once no movement was detected of the given time period. As long as the output is active, any movement detection will be ignored.

2.1.2 Touch button

There are 2 trigger levels to which the capacitive electrode will respond.

The first of these is a Prox event. This event should trigger once the user comes within a small distance to the C_x (in the order of 5cm). This trigger level will not result in an active output, but instead the device will enter Zoom mode. In this mode, the device will sample C_x at 60Hz rather than the selected frequency (f_s) chosen by the designer. This mode switching feature increases the responsiveness of the touch functionality of the device whilst maintaining low power consumption during idle operation.

The second trigger level is a Touch event. This is triggered when the user physically touches the device surface directly above the C_x pad. In the case that the output is inactive during the touch event, the output will be activated. If the touch remains for longer than 500ms the output will start to dim. If a PWM duty of 0% is reached, the duty will start to increase. This

process will continue until the touch is released.

If the output is active when a touch event is registered, the output will be deactivated.

2.2 Metal detection UI

2.2.1 Inductive coil

With a coil connected between the C_{x0} and C_{x1} pins, the IQS680 passes a current through the coil and detects any deviations in the current. The IQS680 interpret these fluctuations in current as the presence or absence of metals, such as copper, in the E-field generated by the current passed through the coil.

If the IQS680 detect metal in close proximity to the coil, the output is deactivated and inversely, if no metal is detected the output is activated.

A second optional capacity measurement is also done on the coil to detect and compensate for any capacitive effect that may be exerted on the coil. This allows the IQS680 to refrain from responding to any touches made on the coil.



2.3 Event output responses

The following figure depicts the responses of the device for all the possible user inputs, given all the possible states of the output.

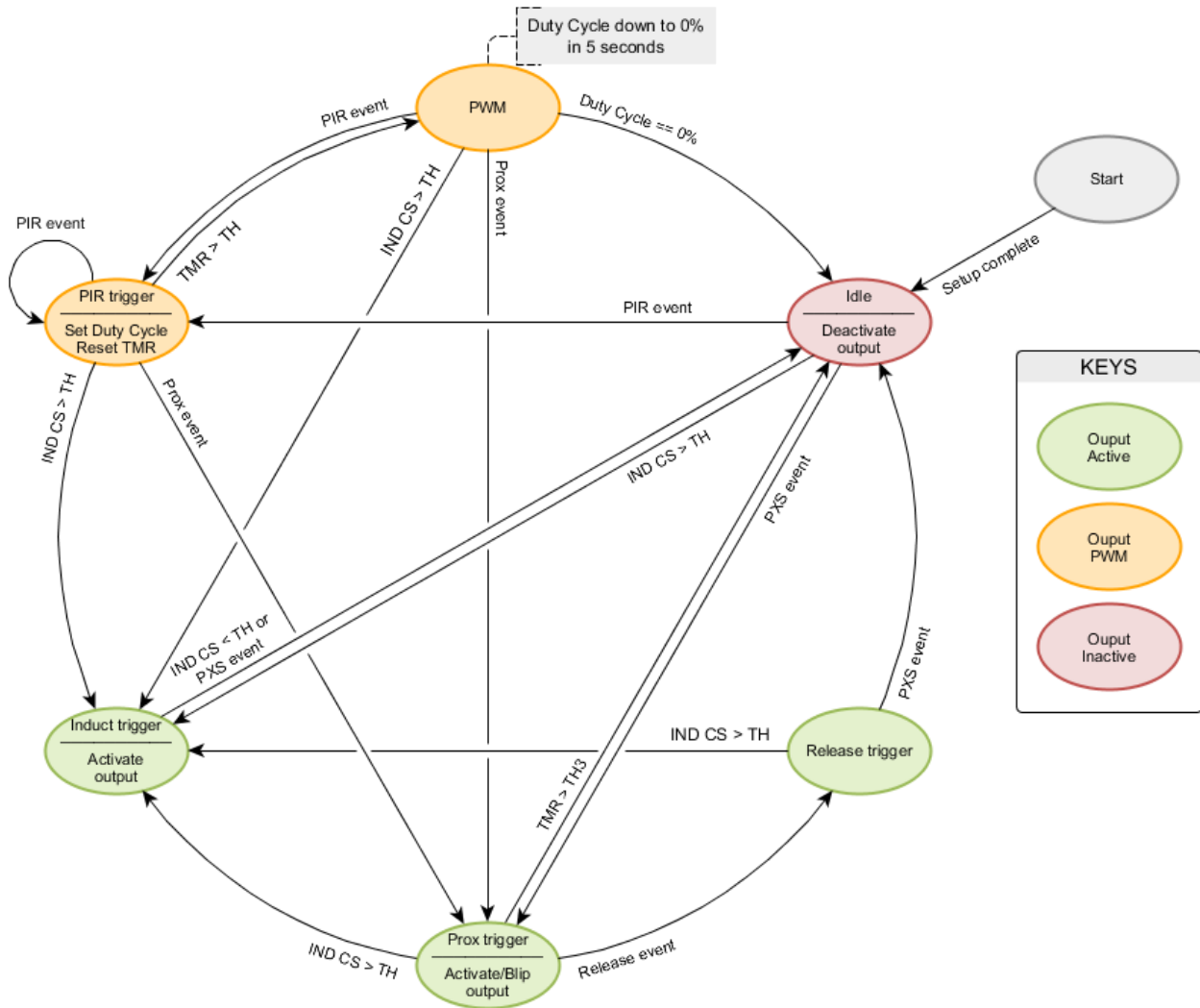


Figure 2.2: State diagram of the IQS680 output



3 Inductive sensing

3.1 Channel specifications

The IQS680 requires 2 sensing lines for inductive sensing. Channel 2 is dedicated to the inductive UI.

Table 3-1 Inductive sensor – channel allocation

Mode	CH0	CH1	CH2
Inductive	○ Touch rejection		● Inductive

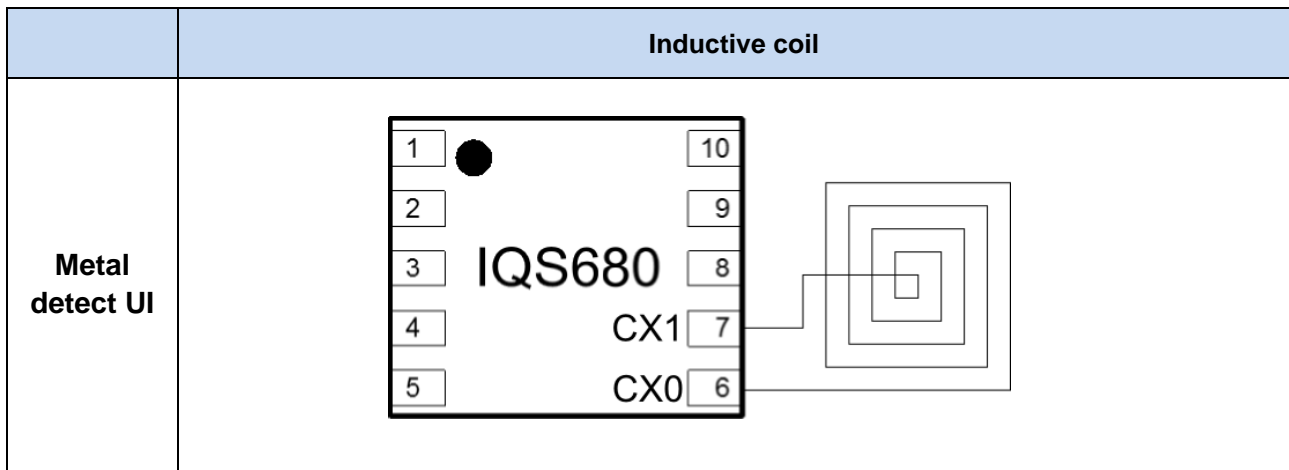
Key:

- - Optional implementation
- - Fixed use for UI

3.2 Hardware configuration

A ferrite bead can be placed in serie with the coil to increase RF immunity.

Table 3-2 Inductive coil hardware description





3.3 Register configuration

3.3.1 Registers to configure for inductive sensing:

Inductive sensing settings registers.

Address	Name	Description	Recommended setting
<u>0x50</u>	Ch0 ProxFusion Settings 0	Sensor mode and configuration.	Sensor mode should be set to Capacitive mode. RX 0 and RX 1 should be enabled and no Tx.
<u>0x52</u>	Ch2 ProxFusion Settings 0	Sensor mode and configuration of each channel.	Sensor mode should be set to Inductive mode. Enable TX1 and RX0
<u>0x53</u>	ProxFusion Settings 1	Global settings for the ProxSense sensors	None
<u>0x54, 0x56</u>	Ch0/Ch2 ProxFusion Settings 2	ATI settings for ProxFusion sensors	ATI target should be more than ATI base to achieve an ATI
<u>0x57</u>	ProxFusion Settings 3	Additional Global settings for ProxFusion sensors	Touch detection enabled
<u>0x60</u>	Proximity Threshold	Proximity Threshold for UI	Less than touch threshold
<u>0x61</u>	Touch Threshold	Touch Threshold for UI	None
<u>0x90</u>	Inductive Prox Threshold	Proximity Threshold for Inductive UI	Less than Enter/Exit Threshold
<u>0x97</u>	Metal Enter NM Threshold	Enter Threshold in non-metal state for Inductive UI	None
<u>0x98</u>	Metal Enter M Threshold	Enter Threshold in metal state for Inductive UI	None
<u>0x99</u>	Metal Exit NM Threshold	Exit Threshold in non-metal state for Inductive UI	None
<u>0x9A</u>	Metal Exit M Threshold	Exit Threshold in metal state for Inductive UI	None



3.4 Sensor data output and flags

The following registers can be monitored by the master to detect inductive sensor related events.

- a) [Event Flags \(0x10\)](#) to prompt for inductive sensor activity. Bit 4 denoted as **IND ENTER** will indicate when a metal object enters the induction sensing area. Bit 5 denoted as **IND EXIT** will indicate when a metal object exits the induction sensing area.

Event Flags (0x10)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read							
Name	SHOW RESET	-	IND EXIT	IND ENTER	-	-	PIR TRIGGER	TOUCH

- b) [Global UI Flags \(0x12\)](#) to prompt for inductive sensor activation. Bit3 denoted as **METAL PRESENT** will indicate the detection of a metal object using the inductive sensing. Bit 6/7 provides the classic prox/touch two level activation outputs.

Global UI Flags (0x12)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read							
Name	METAL PRESENT	TOUCH CH2	PROX CH2	PIR TRIGGER	PIR EVENT	STABLE CH0	TOUCH CH0	PROX CH0

- c) [Channel Counts Ch2 \(0x24 - 0x25\)](#) registers will provide a combined 16-bit value to acquire the magnitude of the inductive sensed object.

Channel counts Ch2 (0x24/0x25)																
Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data Access	Read															
Name	Count High Byte								Count Low Byte							

- d) [Metal Detect Base \(0x34 - 0x35\)](#) registers will provide a combined 16-bit value of the metal detect base value.

Metal Detect Base (0x34/0x35)																
Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data Access	Read															
Name	Metal Detect Base High Byte								Metal Detect Base Low Byte							

Bit definitions:

- Bit 15-0: Base value for metal detection
- e) [Channel 2 LTA \(0x36-0x37\)](#) registers will provide a combined 16-bit value of the LTA of channel 2.

Channel 2 LTA (0x36/0x37)																
Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data Access	Read															
Name	LTA High Byte								LTA Low Byte							

Bit definitions:

- Bit 15-0: LTA filter value



4 Pyroelectric Infrared Radial (PIR) sensing

4.1 Channel Specifications

The IQS680 requires one sensing line for PIR sensing and one sensing line for touch sensing. Channel 1 is dedicated to the PIR UI.

Table 4-1 PIR sensor – channel allocation

Mode	CH0	CH1	CH2
Movement detection	○ Touch	● PIR	

Key:

- - Optional implementation
- - Fixed use for UI

4.2 Hardware Configuration

In the table below are multiple options of configuring sensing (CX) electrodes to realize different implementations.

Table 4-2 PIR hardware description

	Self-capacitive configuration
PIR only	
PIR and touch button	



4.3 Register configuration

4.3.1 Registers to configure for the PIR and capacitive sensing:

PIR and capacitive sensing settings registers

Address	Name	Description	Recommended setting
0x50	Ch0 ProxFusion Settings 0	Sensor mode and configuration.	Sensor mode should be set to capacitive mode. RX 0 should be enabled and no Tx.
0x51	Ch1 ProxFusion Settings 0	Sensor mode and configuration.	Sensor mode should be set to PIR mode. RX 1 should be enabled and no TX.
0x53	ProxFusion Settings 1	Global settings for the ProxSense sensors	None
0x54, 0x55	Ch0/Ch1 ProxFusion Settings 2	ATI settings for ProxFusion sensors	ATI target should be more than ATI base to achieve an ATI
0x57	ProxFusion Settings 3	Additional Global settings for ProxFusion sensors	None
0x60	Proximity threshold	Proximity Threshold for UI	Less than touch threshold
0x61	Touch threshold	Touch Threshold for UI	None
0x90	PIR Settings	PIR Global Settings	Ignore polarity of events
0x91,0x92	PIR Threshold	PIR Event Threshold for UI	PIR Exit Event Threshold ≤ PIR Enter Event Threshold
0x93	PIR Threshold Scale Factor	PIR Threshold Scale Factor for UI	None



4.4 Sensor data output and flags

The following registers can be monitored by the master to detect PIR/touch sensor related events.

- a) [Event Flags \(0x10\)](#) to prompt for PIR or touch sensor activity. Bit 1 denoted as **PIR TRIGGER** will indicate when the PIR is triggered by movement. Bit 0 denoted as **TOUCH** will indicate when the touch sensor is activated.

Event Flags (0x10)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read							
Name	SHOW RESET	-	IND EXIT	IND ENTER			PIR TRIGGER	TOUCH

- b) [Global UI Flags \(0x12\)](#) to prompt for PIR or touch sensor activation. Bit3 denoted as **PIR EVENT** will indicate that a PIR event has occurred. Bit 0/1 provides the classic prox/touch two level activation outputs.

Global UI Flags (0x12)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read							
Name	METAL PRESENT	TOUCH CH2	PROX CH2	PIR TRIGGER	PIR EVENT	STABLE CH0	TOUCH CH0	PROX CH0

- c) [Lighting Flags \(0x13\)](#) to prompt for lighting activity. Bit 4 is set when the PWM output is changing and is cleared when the PWM output is constant. Bit 3 is set when the duty cycle of the PWM output is increasing and is cleared when the duty cycle of the PWM output is decreasing.

Lighting Flags (0x13)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read							
Name	PIR STABLE	PIR RDY	BLIP BUSY	FADING	FADING IN		PIR/IND ACTIVATED	TOUCH ACTIVATED

- d) [Channel Counts \(Raw\) Ch1 \(0x22 - 0x23\)](#) registers will provide a combined 16-bit value of the raw value.

Channel counts Ch1 (0x22-0x23)																
Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data Access	Read															
Name	Count High Byte								Count Low Byte							



- e) **Channel Counts (filtered) Ch1 (0x34 - 0x37)** registers will provide a combined 16-bit value of several filtered values. Channel 1 PDS provides the positive delta sum value. The delta is the difference between the previous sample counts and the current sample counts. Therefore, this value increase if the difference between the previous sample and current sample is positive (counts increasing).

Channel 1 PDS (0x34/0x35)																
Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data Access	Read															
Name	PDS High Byte							PDS Low Byte								

- Bit 15-0: Positive Delta Sum Value

Channel 1 NDS provides the negative delta sum value. The delta is the difference between the previous sample counts and the current sample counts. Therefore, this value increase if the difference between the previous sample and current sample is negative (counts decreasing).

Channel 1 NDS (0x36/0x37)																
Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data Access	Read															
Name	NDS High Byte							NDS Low Byte								

- Bit 15-0: Negative Delta Sim value



5 User Configurable Settings (UCS)

This section describes the user configurable options of the IQS680 in detail. User options are selected through the Azoteq GUI, which is used to write it in the device's EEPROM.

5.1 Sampling frequency

The frequency at which the device samples the sensors directly relates to its power consumption, where a higher sample rate requires a more power. The designer may select 1 of 4 possible sample frequencies as shown in Table 5-1. The sampling frequency can be set in the [Sample Period \(0xD5\) register](#) and [Active Sample Period Adjustment \(0xD4\)](#) registers.

Table 5-1 Sample frequency options

FREQ: Device sampling frequency select	
10 Hz	50 Hz
20 Hz	100 Hz

For a sampling frequency of 10 Hz and 20 Hz a [PIR Filter Beta Value](#) of 2 is recommended and for a sampling frequency of 50 Hz and 100 Hz a [PIR Filter Beta Value](#) of 3 is recommended.

5.2 Input options

The IQS680 includes 3 input modes, which define the sensors attached to the device. The mode can be selected in the [ProxFusion Settings 0 \(0x50-0x53; bits 7-4\)](#) registers. These options are given in the Table 5-2

Table 5-2 User Input options

INPUT: Input type select
PIR sensor only
PIR and capacitive sensors
Coil (metal detect) sensor

5.3 Output format options

The IQS680 includes 4 output formats. These options, given in Table 5-3, allow the designer to operate the load in the best configuration for the given application. The output format can be set in the [System Settings 0 \(0xD2; bits 7&2\)](#) register.

Table 5-3: Output formats

OUTPUT _F : Output format select
Active High & Push-pull
Active Low & Push-pull
Active High & Open-drain
Active Low & Open-drain

5.4 Lighting Modes

The IQS680 includes 3 output modes. These options, given in Table 5-4, allow the designer to operate the load in the best configuration for the given application.



Table 5-4: Output modes

OUTPUT_T : Output mode select
On/Off
Varied PWM
Fixed PWM
Pulse

In the “On/Off” output mode, the IQS680 will always activate the output on any event with a 100% PWM duty. In the “Varied PWM” mode, the IQS680 will cycle through a 0 – 100% PWM duty when a prolonged touch event is detected (longer than 1s), given that the touch event has activated the load. The “Pulse” mode will only generate a short pulse (10us - 250us, selectable in the [Light Time Out \(0xD8\)](#) register) for any event. The output mode can be set in the [System Settings 1 \(0xD3: bits 1-0\)](#) register.

5.5 Auto-off

By default the device’s output will remain in an active state perpetually, given that the output is in a load driven mode. However, if the auto-off feature is selected, the output will be deactivated after a period of 1 hour. The Auto-off bit can be set in the [System Settings 0 \(0xD2; bit 4\)](#) register.

5.6 Proximity threshold

The Proximity Threshold (P_{THR}) defines the minimum required diverges of the Touch CS (CS_T) below the Long Term Average (LTA) for more than 4 consecutive cycles to trigger a proximity event. The IQS680 proximity threshold options range is 0 - 255, where typical values are approximately 8, enabling the designer to obtain the desired sensitivity and noise immunity for the touch electrode. The Proximity Threshold (P_{THR}) can be set in [P Threshold \(0x60\) register](#).

5.7 Touch threshold

Similar to the proximity threshold, the Touch Threshold (T_{THR}) defines the minimum required diverges of the CS_T below the LTA for more than 2 consecutive cycles to trigger a touch event. The following equation illustrates how it is determined whether a touch event has occurred:

$$LTA \times \frac{CS_T}{256} > T_{THR}$$

The IQS680 touch threshold options range is 0 - 255. The touch threshold is selected by the designer to obtain the desired touch sensitivity. The Touch Threshold (T_{THR}) can be set in the [Threshold \(0x61\) register](#).

5.8 PIR event thresholds

Unlike the touch events, which are based on the absolute CS_T measurement, PIR events are based on the differential measurement of the PIR sensor CS (CS_{PIR}). Thus, a PIR Event Threshold (E_{THR}) defines the minimum required *rate* of diverges of CS_{PIR} from its Steady-State CS (CS_{SS}) to trigger a PIR event.

The IQS680 PIR event threshold ranges from 0 - 255, which is chosen to obtain the desired sensitivity and noise immunity for the PIR sensor. A PIR Event is triggered if the Positive Delta Sum (PDS) or Negative Delta Sum (NDS) is greater than the product of the [PIR Threshold Scale Factor \(0x93\)](#) and the [PIR Enter Event Threshold \(0x91\)](#).

$$(PIR_{NDS} \text{ or } PIR_{PDS}) > PIR_{Enter} \times PIR_{Scale}$$



Before another event can be triggered the Positive Delta Sum (PDS) or Negative Delta Sum (NDS) needs to be below the product of the [PIR Threshold Scale Factor \(0x93\)](#) and the [PIR Exit Event Threshold \(0x92\)](#) value.

$$(PIR_{NDS} \text{ or } PIR_{PDS}) < PIR_{Exit} \times PIR_{Scale}$$

[PIR Exit Event Threshold \(0x91\)](#) should be less than or equal to [PIR Enter Event Threshold \(0x92\)](#).

$$PIR_{Enter} \leq PIR_{Exit}$$

5.9 PIR ATI threshold

The PIR sensor is susceptible to ambient noise such as fluctuation in temperature over the course of 24 hours. These changes directly impact the sensitivity of the sensor.

In order to maintain a non-variant sensitivity, the IQS680 will monitor the difference of the CS_{SS} value from the selected ATI target value and compare it to the PIR ATI Threshold (ATI_{THR}) to determine if the device will recalibrate the PIR sensor.

$$CS_{SS} \geq \frac{ATI_{THR}}{255} \times ATI_{Target} ,$$

There are various possible values for ATI_{THR}, some are given in the table below.

Table 5-5: PIR deviation thresholds

ATI _{THR} : PIR ATI THR select	
16	More conservative
24	
32	Less conservative

The PIR ATI threshold can be set in the [Ch1 ATI Threshold \(0x47\)](#) register.

5.10 Number of PIR events

In order to improve the IQS680's resilience against false triggers (important for security applications), the device can be set up to prevent the output from activating until a given number of PIR events has occurred in short succession. The number of events may range from 1 to 4. The number of PIR events can be set in the [PIR Settings 0 \(0x90, bit4-5\)](#) register.

5.11 PIR Trigger Time Out

If a PIR event has occurred, given that the output is in a load driven mode, the device's output will go in an active or PWM state for a selected period. This period can be selected in steps of 4.2 seconds, ranging from 4.2 to 1071 seconds. The PIR Trigger Time Out can be set in [PIR Trigger Time Out \(0xD9\)](#) register.

When a consecutive PIR event occur before the selected period has elapsed, the internal timer will reset and the output will remain active. This implies that the PIR Trigger Time Out defines the time the output will remain active after the last PIR event has occurred.

5.12 Minimum PIR Stabilization Time

Due to the unknown nature of the PIR state at the moment the device receives power, it is necessary for the IQS680 to suppress all PIR events at start-up. The IQS680 automatically monitors the PIR sensor and continue to suppress all PIR events until the sensor has stabilized. This can take up to 30 seconds.

The Minimum PIR stabilization time defines the period which the PIR must be stable before the IQS680 will stop suppressing PIR events. The Minimum PIR Stabilization Time can be set in seconds in the [PIR Time Out Stabilise \(0x95\) register](#).



6 Device clock, power management and mode operation

6.1 Device main oscillator

The IQS680 has an **8MHz** main oscillator to clock all system functionality. The ProxFusion® channels charges at half of the main oscillator frequency. Therefore, the frequency multiplier selected in [ProxFusion Settings 1 \(0x53; bit 4-5\)](#) is multiplied by half of the main oscillator frequency.

6.2 Device modes

The IQS680 supports the following modes of operation;

- **Active Power mode** (Increased report rate)
- **Low Power mode** (Fixed report rate)

The device will automatically switch between the different operating modes. The IQS680 is in a permanent low-power mode until the output is activated by an event. When the IQS680 switches to Active Power mode the Output Active flag will be set in the [System Flags \(0x11; bit 7\)](#) register.

6.2.1 Active Power mode

Active Power mode is the fully active sensing and load driving mode to function when an event has activated the output. A sample period adjustment can be specified in the [Active Sample Period Adjustment \(0xD4\)](#) register. The designer may select 1 of 4 possible sample frequencies as shown in Table 5-1.

6.2.2 Low Power mode

Low Power mode is the fully active sensing mode to function at a fixed report rate specified in the [Sample Period \(0xD5\)](#) register. The designer may select 1 of 4 possible sample frequencies as shown in Table 5-1. Reduced report rates also reduce the current consumed by the sensor.

6.2.3 Active time

The amount of time the IQS680 is in active power mode is determined by the [PIR Trigger Time Out \(0xD9\)](#). The PIR Trigger flag will be cleared after this time and the IQS680 will enter Low Power Mode.

6.3 Streaming and Standalone mode:

Standalone mode is the default. Streaming mode can be enabled by writing to the EEPROM as explained in [Chapter 8](#) or by using the GUI.

6.3.1 Streaming mode

The ready is triggered every cycle and per the report rate. Data can be streamed or settings can be changed using the I2C communication interface.

6.3.2 Standalone mode

The ready is triggered only when an event has occurred.

Settings stored on the EEPROM are loaded at POR. The device operates in standalone mode without the need for an MCU

The events which trigger the ready:

- PIR event trigger
- Touch or proximity events on channel 0 or 2

Note: Both these events have built in hysteresis which filters out very slow changes



7 Communication

The **IQS680** device interfaces to a master controller via a 3-wire (SDA, SCL and RDY) serial interface bus that is I²C™ compatible with a maximum communication speed of 400 kHz. The communications interface of the IQS680 supports the following:

- Streaming data as well as standalone mode.
- The master may address the device at any time (if in streaming mode). If the IQS680 is not in a communication window, the device returns an ACK after which clock stretching is induced until a communication window is entered. Additional communication checks are included in the main loop to reduce the average clock stretching time.
- The provided interrupt line (RDY) is open-drain **active high** implementation and indicates a communication window.

7.1 Control Byte

The Control byte indicates the 7-bit device address (44H default) and the Read/Write indicator bit. The structure of the control byte is shown in Figure 7.1.

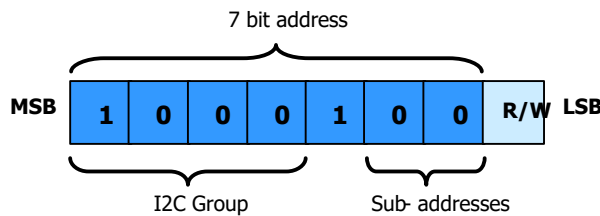


Figure 7.1: IQS680 Control Byte

The I²C device has a 7-bit Slave Address (default 0x44H) in the control byte as shown in 0. To confirm the address, the software compares the received address with the device address. Sub-address values can be set by OTP programming options.

7.2 I²C Read

To read from the device a *current address read* can be performed. This assumes that the address-command is already setup as desired.

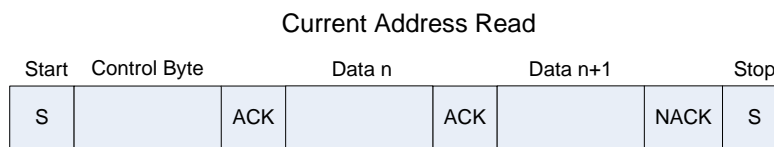


Figure 7.2: Current Address Read

If the address-command must first be specified, then a *random read* must be performed. In this case a WRITE is initially performed to setup the address-command, and then a repeated start is used to initiate the READ section.

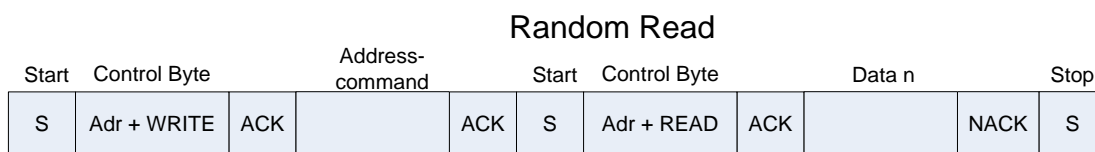


Figure 7.3: Random Read



7.3 I²C Write

To write settings to the device a *Data Write* is performed. Here the Address-Command is always required, followed by the relevant data bytes to write to the device.

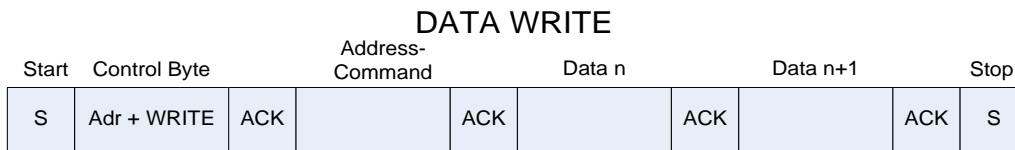


Figure 7.4: I²C Write.

7.4 End of Communication Session / Window

Similar to other Azoteq I²C devices, to end the I²C communication session, a STOP command is given. When sending numerous read and write commands in one communication cycle, a repeated start command must be used to stack them together (since a STOP will jump out of the communication window, which is not desired).

The STOP will then end the communication, and the IQS680 will return to process a new set of data. Once this is obtained, the communication window will again become available (RDY set LOW).

7.5 Device address and sub-addresses

The default device address is **0x44 = DEFAULT_ADDR**.

Alternative sub-address options are definable in the following one-time programmable bits:
OTP Bank2 (bit0-bit7) = SUB_ADDR_0 to SUB_ADDR_255.

- a) Default address: 0x44 = DEFAULT_ADDR (0x44) **OR** SUB_ADDR_0 (00000000b)
- b) Sub-address: 0x45 = DEFAULT_ADDR (0x44) **OR** SUB_ADDR_1 (00000001b)
- c) Sub-address: 0x46 = DEFAULT_ADDR (0x44) **OR** SUB_ADDR_2 (00000010b)
- d) Etc.

7.6 Additional OTP options

All one-time-programmable device options are located in FG bank 3.

Floating Gate Bank3								
Bit Number	7	6	5	4	3	2	1	0
Name	Reserved						I2C slave	EEPROM Read
Default	XX	XX	XX	XX	XX	XX	0	1

Bit definitions:

- Bit 0: EEPROM Read
 - 0: Disable EEPROM Read
 - 1: Enable EEPROM Read
- Bit 1: I2C slave
 - 0: Standalone/GPIO mode
 - 1: I2C enabled on IQS680
- Bit 2-7: Reserved
 - XX: Do not change these bits. The IQS680 will not function properly.



7.7 I²C Specific Commands

7.7.1 Show Reset

After start-up, and after every reset event, the “Show Reset” flag will be set in the [Event Flags register \(0x10; bit 7\)](#).

The “Show Reset” bit can be read to determine whether a reset has occurred on the device (it is recommended to be continuously monitored). This bit will be set '1' after a reset.

The “Show Reset” flag will be cleared (set to '0') by writing a '1' into the “Ack Reset” bit in the [I²C Command register \(0xD0; bit 0\)](#) . A reset will typically take place if a timeout during communication occurs.

7.8 I²C I/O Characteristics

The **IQS680** requires the input voltages given in Table 7-1, for detecting high (“1”) and low (“0”) input conditions on the I²C communication lines (SDA, SCL and RDY).

Table 7-1 IQS680 I²C Input voltage

	Input Voltage (V)
V _{inLOW}	0.3*VDDHI
V _{inHIGH}	0.7*VDDHI

Table 7-2 provides the output voltage levels of the **IQS680** device during I²C communication.

Table 7-2 IQS680 I²C Output voltage

	Output Voltage (V)
V _{outLOW}	GND +0.2 (max.)
V _{outHIGH}	VDDHI – 0.2 (min.)

7.9 Recommended communication and runtime flow diagram

The following is a basic master program flow diagram to communicate and handle the device when in streaming mode. It addresses possible device events such as output events, ATI and system events (resets).

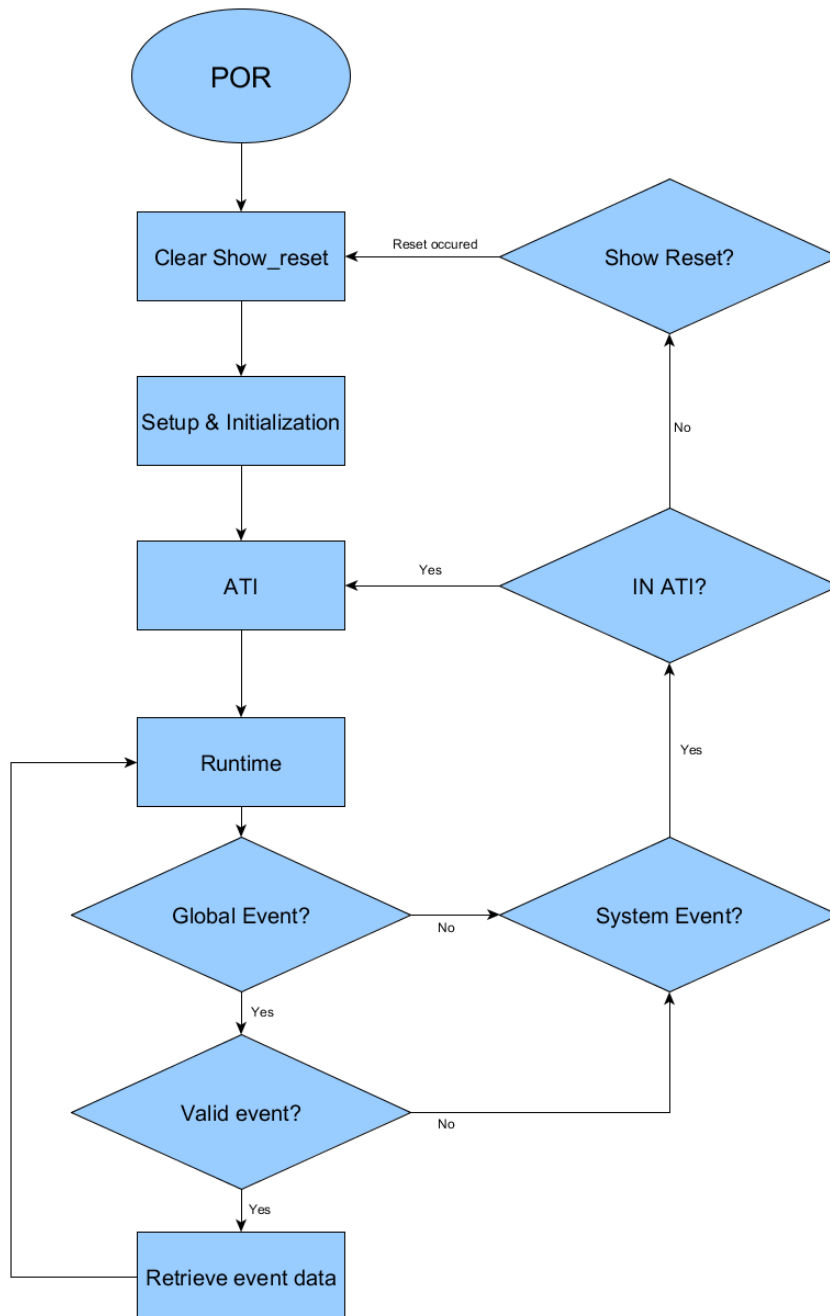


Figure 7.5 Master command structure and runtime event handling flow diagram

It is recommended that the master verifies the status of the Flag Registers (0x10 – 0x13) bits to identify events and resets. Detecting either one of these should prompt the master to the next steps of handling the IQS680.

Streaming mode communication is used for detail sensor evaluation during prototyping and/or development phases.

Standalone mode communication is recommended for runtime use of the IQS680. Streaming mode communication is used for detail sensor evaluation during prototyping/development.



8 Writing to the EEPROM

The IQS680 has an EEPROM included on-chip for calibration data and settings. Device settings can be written to the EEPROM at power-on. To ensure that the correct data is written to the EEPROM the IQS680 should be in Test Mode (TM). The EEPROM used in the IQS680 is the FT24C02A, for further information regarding communication with the EEPROM please see the FT24C02A datasheet.

8.1 EEPROM and the IQS680

The EEPROM is used to store the settings for each IC. The master can either write to the EEPROM or the IQS680 to change settings. The EEPROM will store these settings and the IQS680 will automatically load these settings on power up. Writing to the EEPROM requires a power cycle for the IQS680 to read these settings. To change settings on-the-fly or read data from the IQS680 the master should communicate with the IQS680 (RAM) and not the EEPROM.

8.2 EEPROM Structure

Table 8-1 shows the values that must be written to the EEPROM in hexadecimal format. The 1st row indicates the lower nibble and the 1st column gives the higher nibble of the of the EEPROM register address. That is, the register with address 0x36 is found in row 3, column 6 and has the value 0x5F.

The first two bytes indicates the size of the EEPROM to the IQS680 and should not be changed. Only the values indicated in Table 8-1 should be written. Each register is written in pairs of two in the EEPROM. The first byte should not be changed and the second byte (in green) is the value of the register. The user can only change the values indicated in green. Default values for PIR initialisation is given in Table 8-1. The description of each register can be found in the [IQS680 Register Map](#) in Section 9. For example, EEPROM register 0x26-0x27 holds the data for the Prox Threshold Ch0 register. The value in 0x26 is used by the IQS680 and may not be changed. The value in 0x27 may be changed to increase/decrease the Prox Threshold.

8.3 How to write to the EEPROM

The IQS680 should be in TM to write settings to the EEPROM. To enter TM the master should poll the IQS680 by reading from the address 0x0F. If the IQS680 returns 0xA5 the device is in TM. The master should start polling the IQS680 within 10 ms after the IQS680 has received power to enter TM.

The EEPROM should be written in rows of 16 bytes. Therefore, only one row can be written at a time. The IQS680 is by default in standalone mode. To change to I2C mode the [floating gate in bank 3](#) is read without issuing an I2C stop command. The reserved bits should not be changed and the I2C bit should be set. To enable writing to the EEPROM the master should read 0xA6 from 0xE4. Once the IQS680 is in TM and EEPROM writing is enabled the master can write to the EEPROM address (0x50). Short delays are required in between page writing to allow the EEPROM to successfully store the data.

Sample code is given in [Appendix A: EEPROM Sample Code](#). If the master has successfully written to the EEPROM, a power cycle will ensure that the IQS680 reads the EEPROM on power up. Table 8-2 explains the process to follow.



Table 8-1: Data in Hexadecimal values that should be written to EEPROM

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	2B	13	XX	E8	00	E9	00	EA	00	F0	00	F1	00	F2	00
	Size		FG_BYTE3		Ch0 Comp		Ch1 Comp		Ch2 Comp		Ch0 Multipliers		Ch1 Multipliers		Ch2 Multipliers	
1	7D	14	7E	20	7F	0F	F3	01	F4	92	F5	00	F6	63	F7	8A
	Ch0 ATI Threshold		Ch1 ATI Threshold		Ch2 ATI Threshold		ProxFusion Settings 0_0		ProxFusion Settings 0_1		ProxFusion Settings 0_2		ProxFusion Settings 1		ProxFusion Settings 2_0	
2	F8	59	F9	60	FA	05	98	0A	99	14	9A	01	FB	10	FC	0A
	ProxFusion Settings 2_1		ProxFusion Settings 2_2		ProxFusion Settings 3		Prox Threshold Ch0		Touch Threshold Ch0		Stable Threshold Ch0		Prox Halt Time		Touch Halt Time	
3	C8	4B	C9	01	CA	01	5F	10	BE	23	BF	0	BC	10	1C	83
	PIR Settings		PIR Exit Event Threshold		PIR Enter Event Threshold		PIR Threshold Scale Factor		ATI Time Out PIR		Block Time Out PIR		Stabilise Time Out PIR		Active Channels	
4	17	44	18	80	16	00	CB	04	57	06	BB	00	BD	01	DF	FF
	System Settings 0		System Settings 1		Active Sample Period Adjustment		Sample Period		I2C Time Out		Light Time Out		PIR Trigger Time Out		PWM Duty Cycle	
5	A8	06	A9	04	AA	04	AB	06	FF	FF	FF	FF	FF	FF	FF	FF
	Metal Enter NM Threshold		Metal Enter M Threshold		Metal Exit NM Threshold		Metal Exit M Threshold									
6	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
7	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
8	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
9	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
A	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
B	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
C	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
D	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF
E	0	0	0	0	FF	FF	FF	FF	FF	XX	XX	XX	XX	XX	XX	XX
F	0	0	0	0	FF	FF	FF	FF	FF	XX	XX	XX	XX	XX	XX	XX

The registers marked with a value of “XX” are values that are calculated at FT and should not be changed. Only change registers in green.

Table 8-2: How to write to EEPROM

Enter Test Mode				Read Floating Gate				Enable EEPROM Write				
Start	IQS680 Adr	Read Adr	Data Receive	Start	IQS680 Adr	Read Adr	Data Receive	Start	IQS680 Adr	Read Adr	Data Receive	Stop
S	0x44	0x0F	0xA5	S	0x44	0x13	XX	S	0x44	0xE4	0xA6	S

Write to EEPROM						Power Cycle
Start	EEPROM Adr	Page Adr	Data(n)	Data(n+1)	Stop	
S	0x50				S	



9 IQS680 Register Map

Table 9-1 IQS680 Register map

Register Address	Group	Register Name
00H	Device Information	Product Number
01H		Software Number
02H		Hardware Number
10H	Device Specific Data	Event Flags
11H		System Flags
12H		Global UI Flags
13H		Lighting Flags
20H	Channel Counts (raw data)	CH0 CS Low (Touch/ Inductive)
21H		CH0 CS High (Touch/ Inductive)
22H		CH1 CS Low (PIR)
23H		CH1 CS High (PIR)
24H		CH2 CS Low (Inductive)
25H		CH2 CS High (Inductive)
30H	Channel Counts (filtered data)	CH0 LTA Low (Touch/ Inductive)
31H		CH0 LTA High (Touch/ Inductive)
34H		CH1 PDS Low (PIR) / Metal Detect Base Low (Inductive)
35H		CH1 PDS High (PIR) / Metal Detect Base High (Inductive)
36H		CH1 NDS Low (PIR) / CH2 LTA Low (Inductive)
37H		CH1 NDS High (PIR) / CH2 LTA High (Inductive)
40H	ProxFusion Sensor Settings 0	Ch0 Compensation
41H		Ch1 Compensation
42H		Ch2 Compensation
43H		Ch0 Multipliers
44H		Ch1 Multipliers
45H		Ch2 Multipliers
46H		Ch0 ATI Threshold
47H		Ch1 ATI Threshold
48H		Ch2 ATI Threshold
50H	ProxFusion Sensor Settings 1	ProxFusion Settings 0_0
51H		ProxFusion Settings 0_1
52H		ProxFusion Settings 0_2
53H		ProxFusion Settings 1
54H		ProxFusion Settings 2_0
55H	ProxFusion Settings 2_1	
56H	ProxFusion Sensor Settings 1	ProxFusion Settings 2_2
57H		ProxFusion Settings 3
60H	ProxFusion UI Settings	Prox Threshold Ch0
61H		Touch Threshold Ch0
62H		Stable Threshold Ch0



Register Address	Group	Register Name
63H		Prox Halt Time
64H		Touch Halt Time
90H	Inductive UI Settings	Inductive Prox Threshold
97H		Metal Enter NM Threshold
98H		Metal Enter M Threshold
99H		Metal Exit NM Threshold
9AH		Metal Exit M Threshold
9BH		PIR Settings
90H	PIR Sensor Settings	PIR Exit Event Threshold
91H		PIR Enter Event Threshold
92H		PIR Threshold (Scale Factor)
93H		Re-ATI Time Out PIR
94H		Block Time Out PIR
95H		Stabilise Time Out PIR
96H		I²C Command
D0H	Device and Power mode Settings	Active Channels
D1H		System Settings 0
D2H		System Settings 1
D3H		Active Sample Period Adjustment
D4H		Sample Period
D5H		I2C Time Out
D7H		Light Time Out
D8H		PIR Trigger Time Out
D9H		PWM Value
F8H		PWM Duty Cycle



9.1 Device Information Data

9.1.1 Product Number

Product Number (0x00)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read							
Name	Device Product Number							

- Bit 0-7: Device Product Number = D'71'

9.1.2 Software Number

Hardware Number (0x01)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read							
Name	Device Hardware Number							

- Bit 0-7: Device Hardware Number = D'131'

9.1.3 Hardware Number

Software Number (0x02)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read							
Name	Device Software Number							

- Bit 0-7: Device Software Number = D'32'

9.2 Device Specific Data

9.2.1 Event Flags

Event Flags (0x10)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read							
Name	SHOW RESET	-	IND EXIT	IND ENTER	-	-	PIR TRIGGER	TOUCH

Bit definitions:

- Bit 7: Reset Indicator:
 - 0: No reset event
 - 1: A device reset has occurred and needs to be acknowledged
- Bit 5: Induction Exit:
 - 0: No event to report
 - 1: Metal has been removed from the IC
- Bit 4: Induction Enter:
 - 0: No event to report
 - 1: Metal has been added to the IC
- Bit 1: PIR Trigger:
 - 0: No event to report
 - 1: A PIR event has occurred
- Bit 0: ProxSense / Capacitive Sensing Touch indicator:
 - 0: No event to report
 - 1: A touch event has occurred



9.2.2 System Flags

System Flags (0x11)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read							
Name	OUTPUT ACTIVE	-	PIR STABLE	-	-	-	IN ATI	IN ZOOM

Bit definitions:

- Bit 7: Output Active:
 - 0: No event to report
 - 1: Load activated by UI event
- Bit 5: PIR Stabilized:
 - 0: Indicate that PIR has not stabilized
 - 1: Indicate that PIR has stabilized
- Bit 1: ATI Busy Indicator:
 - 0: No channels are in ATI
 - 1: One or more channels are in ATI
- Bit 0: Zoom mode indicator:
 - 0: No event to report
 - 1: Indicates that the PIR is in zoom mode

9.2.3 Global UI Flags

Global UI Flags (0x12)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read							
Name	METAL PRESENT	TOUCH CH2	PROX CH2	PIR TRIGGER	PIR EVENT	STABLE CH0	TOUCH CH0	PROX CH0

Bit definitions:

- Bit 7: Metal Present flag:
 - 0: No Metal
 - 1: Metal Detected
- Bit 6: Channel 2 touch indicator:
 - 0: Channel 2 delta below touch threshold
 - 1: Channel 2 delta above touch threshold
- Bit 5: Channel 2 prox indicator:
 - 0: Channel 2 delta below prox threshold
 - 1: Channel 2 delta above prox threshold
- Bit 4: Trigger event indicator:
 - 0: No event to report
 - 1: A PIR trigger event has occurred
- Bit 3: PIR event indicator:
 - 0: No event to report
 - 1: Indicates that a PIR event has occurred
- Bit 2: Channel 0 stability indicator:
 - 0: Channel 0 is not stable
 - 1: Indicates that channel 0 is stable
- Bit 1: Touch indicator:
 - 0: Channel 0 delta below touch threshold
 - 1: Channel 0 delta above touch threshold
- Bit 0: Channel 0 prox indicator:
 - 0: Channel 0 delta below prox threshold
 - 1: Channel 0 delta above prox threshold



9.2.4 Lighting Flags

Lighting Flags (0x13)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read							
Name	PIR STABLE	PIR RDY	BLIP BUSY	<u>FADING</u>	<u>FADING IN</u>	-	PIR/IND ACTIVATED	TOUCH ACTIVATED

Bit definitions:

- Bit 7: PIR Stabilized:
 - 0: Indicate that PIR has not stabilized
 - 1: Indicate that PIR has stabilized
- Bit 6: PIR not Ready indicator:
 - 0: PIR events can occur
 - 1: PIR events are blocked
- Bit 5: BLIP busy indicator:
 - 0: PIR event indicator inactive
 - 1: PIR event indicator active
- Bit 4: Fading indicator:
 - 0: Load PWM duty cycle is constant
 - 1: Load PWM duty cycle is changing
- Bit 3: Fading in indicator:
 - 0: PWM Duty cycle decrease
 - 1: PWM Duty cycle increase
- Bit 1: PIR/Induction light activation:
 - 0: No event to report
 - 1: Indicates that the light is activated by a PIR or induction event
- Bit 0: Touch event activation
 - 0: No event to report
 - 1: Indicates that the light is activated by a touch event

9.3 Channel Counts (raw data)

Channel counts Ch0/1/2/3 (0x20/0x21-0x26/0x27)																
Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data Access	Read															
Name	Count High Byte								Count Low Byte							

- Bit 15-0: Raw or AC Filter data

9.4 Channel Counts (filtered data)

9.4.1 Channel 0 LTA

Channel 0 LTA (0x30/0x31)																
Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data Access	Read															
Name	LTA High Byte								LTA Low Byte							

- Bit 15-0: LTA filter Value

9.4.2 Channel 1 PDS / Metal Detect Base

Note: Registers 0x34 and 0x35 are shared between the Inductive UI and PIR UI. These UI's cannot be enabled at the same time.



9.4.2.1 PIR UI

Channel 1 PDS (0x34/0x35)																
Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data Access	Read															
Name	PDS High Byte								PDS Low Byte							

- Bit 15-0: Positive Delta Sum Value

9.4.2.2 Inductive UI

Metal Detect Base (0x34/0x35)																
Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data Access	Read															
Name	Metal Detect Base High Byte								Metal Detect Base Low Byte							

- Bit 15-0: Base value for metal detection

9.4.3 Channel 1 NDS / Channel 2 LTA

Note: Registers 0x36 and 0x37 are shared between the Inductive UI and PIR UI. These UI's cannot be enabled at the same time.

9.4.3.1 PIR UI

Channel 1 NDS (0x36/0x37)																
Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data Access	Read															
Name	NDS High Byte								NDS Low Byte							

- Bit 15-0: Negative Delta Sum value

9.4.3.2 Inductive UI

Channel 2 LTA (0x36/0x37)																
Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data Access	Read															
Name	LTA High Byte								LTA Low Byte							

- Bit 15-0: LTA filter value

9.5 ProxFusion Sensor Settings block 0

9.5.1 Compensation

Compensation Ch0,1,2 (0x40-0x42)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	Compensation (7-0)							

- Bit 7-0: Lower 8 bits of the Compensation Value (0-255)

9.5.2 Multipliers

Multipliers values Ch0,1,2 (0x43-0x45)									
Bit Number	7	6	5	4	3	2	1	0	
Data Access	Read/Write								
Name	Compensation (9-8)		Coarse multiplier			Fine multiplier			

Bit definitions:

- Bit 7-6: Compensation upper two bits
 - 0-3: Upper 2-bits of the Compensation value.
- Bit 5-4: Coarse multiplier Selection:



- 0-3: Coarse multiplier selection
- Bit 3-0: Fine Multiplier Selection:
 - 0-15: Fine Multiplier selection

9.5.3 ATI Threshold

ATI Threshold Ch0,1,2 (0x46-0x48)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	ATI Threshold (0-255)							
Default (0x46)								

- Bit 7-0: ATI Threshold Value

9.6 ProxFusion Sensor Settings block 1

9.6.1 ProxFusion Settings 0

9.6.1.1 PIR/Capacitive sensing

ProxFusion Settings 0_0 (0x50)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	Sensor mode			TX select		RX select		
Default	01H							

Bit definitions:

- Bit 7-4: Sensor mode select:
 - 0000: Self capacitive mode
- Bit 3-2: TX-select:
 - 00: TX 0 and TX 1 are disabled
- Bit 1-0: RX select:
 - 01: RX 0 is enabled

ProxFusion Settings 0_1 (0x51)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	Sensor mode			TX select		RX select		
Default	92H							

Bit definitions:

- Bit 7-4: Sensor mode select:
 - 1001: PIR mode
- Bit 3-2: TX-select:
 - 00: TX 0 and TX 1 are disabled
- Bit 1-0: RX select:
 - 10: RX 1 is enabled

9.6.1.2 Inductive sensing

ProxFusion Settings 0_0 (0x50)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	Sensor mode			TX select		RX select		
Default	03H							

Bit definitions:



- Bit 7-4: Sensor mode select:
 - 0000: Self capacitive mode
- Bit 3-2: TX-select:
 - 00: TX 0 and TX 1 are disabled
- Bit 1-0: RX select:
 - 11: RX 0 and RX 1 are enabled

ProxFusion Settings 0_2 (0x52)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	Sensor mode			TX select			RX select	
Default	29H							

Bit definitions:

- Bit 7-4: Sensor mode select:
 - 0010: Self Inductive mode
- Bit 3-2: TX-select:
 - 10: TX 1 is enabled
- Bit 1-0: RX select:
 - 01: RX 0 is enabled

9.6.2 ProxFusion Settings 1

ProxFusion Settings 1 (0x53)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	-	CS PXS	Charge Freq	Proj bias			Auto ATI Mode	

Bit definitions:

- Bit 6: ProxFusion / Capacitive Sensing Capacitor size select:
 - 0: ProxFusion storage capacitor size is 15 pF
 - 1: ProxFusion storage capacitor size is 60 pF
- Bit 5-4: Charge Frequency select:
 - 00: 1/2
 - 01: 1/4
 - 10: 1/8
 - 11: 1/16
- Bit 3-2: Projected bias:
 - 00: 2.5 μ A
 - 01: 5 μ A
 - 10: 10 μ A
 - 11: 20 μ A
- Bit 1-0: Auto ATI Mode select:
 - 00: ATI Disabled
 - 01: Partial ATI (Multipliers are fixed)
 - 10: Semi Partial ATI (Coarse multipliers are fixed)
 - 11: Full ATI



9.6.3 ProxFusion Settings 2

ProxFusion Settings 2 (0x54-0x56)									
Bit Number	7	6	5	4	3	2	1	0	
Data Access	Read/Write								
Name	ATI Base			ATI Target					

Bit definitions:

- Bit 7-6: ATI Base value select:
 - 00: 75
 - 01: 100
 - 10: 150
 - 11: 200
- Bit 5-0: ATI Target:
 - ATI Target is 6-bit value x 32

9.6.4 ProxFusion Settings 3

ProxFusion Settings 3 (0x57)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	-	-	IGNORE TOUCH	-	LTA BETA		ACF BETA	

Bit definitions:

- Bit 5: Touch Detection
 - 0: Touch detection enabled
 - 1: Touch detection disabled
- Bit 3-2: LTA Beta Value
 - 00: 7
 - 01: 8
 - 10: 9
 - 11: 10
- Bit 1-0: AC Filter Beta Value
 - 00: 1
 - 01: 2
 - 10: 3
 - 11: 4

9.7 ProxFusion UI Settings

9.7.1 Prox Threshold Channel 0

Proximity Threshold Ch0 (0x60)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	Proximity Threshold							

- Bit 7-0: Proximity threshold value (0-255)

If a difference between the LTA and counts value would exceed this threshold the proximity event would be flagged.



9.7.2 Touch Threshold Channel 0

Touch Threshold Ch0 (0x61)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	Touch Threshold							

- Bit 7-0: Touch Threshold (0-255) = Touch threshold value * LTA/ 256

If a difference between the LTA and counts value would exceed this threshold the touch event would be flagged.

9.7.3 Stable Threshold Channel 0

Stable Threshold Ch0 (0x62)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	Stable Threshold							

- Bit 7-0: Stable threshold value (0-255)

9.7.4 Prox Halt Time

Prox Halt Time (0x63)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	Prox Halt Time							

- Bit 7-0: Prox halt time in 260ms increments ((0-255) x 260ms)

9.7.5 Touch Halt Time

Touch Halt Time (0x64)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	Touch Halt Time							

- Bit 7-0: Touch halt time in 260ms increments ((0-255) x 260ms)

9.8 Inductive UI Settings

Note: Registers 0x90, 0x97, 0x98, 0x99, 0x9A are shared between the Inductive UI and PIR UI. These UI's cannot be enabled at the same time.

9.8.1 Inductive Prox Threshold

Inductive Prox Threshold (0x90)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	Prox Threshold							

- Bit 7-0: Proximity threshold value (0-255)

9.8.2 Metal Enter NM Threshold

Metal Enter NM Threshold (0x97)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	Threshold							



- Bit 7-0: Threshold value (0-255)

This threshold value is used to detect when metal enters the sensor area if the IC is in a non-metal state.

9.8.3 Metal Enter M Threshold

Metal Enter M Threshold (0x98)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	Threshold							

- Bit 7-0: Threshold value (0-255)

This threshold value is used to detect when metal enters the sensor area if the IC is in a metal state.

9.8.4 Metal Exit NM Threshold

Metal Exit NM Threshold (0x99)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	Threshold							

- Bit 7-0: Threshold value (0-255)

This threshold value is used to detect when metal exits the sensor area if the IC is in a non-metal state.

9.8.5 Metal Exit M Threshold

Metal Exit M Threshold (0x9A)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	Threshold							

- Bit 7-0: Threshold value (0-255)

This threshold value is used to detect when metal exits the sensor area if the IC is in a metal state.

9.9 PIR Sensor Settings

Note: Registers 0x90, 0x97, 0x98, 0x99, 0x9A are shared between the Inductive UI and PIR UI. These UI's cannot be enabled at the same time.

9.9.1 PIR Settings

PIR Settings (0x90)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	IS POLAR	-	NR OF EVENTS	UTH TRIGGER BLOCK		BETA		
Default	43H							

Bit definitions:

- Bit 7: Polar Selection:
 - 0: Ignores polarity of PIR events
 - 1: Alternating positive/negative events
- Bit 5-4: Specify the number of events before PIR trigger:
 - 00: 1 Event before trigger
 - 01: 2 Events before trigger
 - 10: 3 Events before trigger



- 11: 4 Events before trigger
- Bit 3: Trigger Block
 - 0: Accepts very big events
 - 1: Ignores very big PIR events
- Bit 2-0: PIR Filter Beta Value (1-7) ([3 or 2 recommended](#))

9.9.2 PIR Exit Event Threshold

PIR Exit Event Threshold (0x91)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	PIR Exit Event Threshold Value							

- Bit 15-0: [PIR Exit Event Threshold Value](#) (0-255) should be smaller than or equal to [PIR Enter Event Threshold Value](#)

9.9.3 PIR Enter Event Threshold

PIR Enter Event Threshold (0x92)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	PIR Enter Event Threshold Value							

- Bit 15-0: [PIR Enter Event Threshold Value](#) (0-255)

9.9.4 PIR Threshold Scale Factor

PIR Threshold Scale Factor (0x93)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	PIR Threshold Scale Factor							

- Bit 7-0: [PIR Threshold Scale Factor](#) (0-255)

9.9.5 ATI Time Out PIR

ATI Halt Time Out PIR (0x94)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	ATI Halt Time Out Period							

- Bit 7-0: ATI Halt Time Out Period in 260 ms ticks ((0-255) x 260 ms)

9.9.6 Block Time Out PIR

Block Time Out PIR (0x95)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	Block Time Out Period				Minimum Trigger Period			

Bit definitions:

- Bit 3-0: Minimum period the PIR will remain triggered after a PIR event in 260ms ticks ((0-15) x 260 ms).
- Bit 7-4: The period the PIR is blocked after the LED has switched off for Block Time Out Period in 260ms ticks Period ((0-15) x 260 ms).



9.9.7 Stabilise Time Out PIR

Stabilise Time Out PIR (0x96)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	Stabilise Time Out Period							

- Bit 7-0: Maximum stabilise time in 260 ms ticks ((0-255) x 260 ms)

9.10 Device and Power Mode Settings

9.10.1 I²C Command

I ² C Command (0xD0)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	-	-	-	-	SET REDO ATI	RESEED	SOFT RESET	ACK RESET

Bit definitions:

- Bit 3: Redo ATI on channels (Set only, will clear when done)
 - 1 – Start the ATI process
- Bit 2: Reseed All Long-term filters (Set only, will clear when done)
 - 1 – Start the Reseed process
- Bit 1: Soft Reset (Set only, will clear when done)
 - 1 – Causes the device to perform a software reset
- Bit 0: Acknowledge reset (Set only, will clear when done)
 - 1 – Acknowledge that a reset has occurred. This event will trigger until acknowledged

9.10.2 Active Channels

Active channels mask (0xD1)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	-	-	-	-	-	CH2	CH1	CH0

Bit definitions:

- Bit 2: CH2 (Induction)
 - 0: Channel 2 is disabled
 - 1: Channel 2 is enabled
- Bit 1: CH1 (PIR)
 - 0: Channel 1 is disabled
 - 1: Channel 1 is enabled
- Bit 0: CH0 (Touch/Inductive)
 - 0: Channel 0 is disabled
 - 1: Channel 0 is enabled

9.10.3 System Settings 0

System Settings 0 (0xD2)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	OUTPUT ACTIVE HIGH	VREG ON	LED OFF	AUTO OFF	-	OUTPUT PP	-	ACF DISABLE

Bit definitions:

- Bit 7: Output Format 0
 - 0: Output is active low
 - 1: Output is active high



- Bit 6: Enable VReg when in ULP
 - 0: VReg disabled when in ULP
 - 1: VReg enabled when in ULP
- Bit 5: LED Off Block
 - 0: LED does not indicate when PIR events are blocked
 - 1: LED will indicate when PIR events are blocked
- Bit 4: Enable Light Auto Off
 - 0: Light stays on when time out
 - 1: Light switches off on timeout
- Bit 2: Output Format 1
 - 0: Open-drain format
 - 1: Push-pull format
- Bit 0: AC Filter Enable
 - 0: AC filter enabled
 - 1: AC filter disabled

9.10.4 System Settings 1

System Settings 1 (0xD3)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	BLOCK PIR ON LED	-	-	-	-		LIGHTING MODE	

Bit definitions:

- Bit 7: Block PIR on LED
 - 0: PIR is not blocked when LED switches off
 - 1: PIR is blocked when LED switches off for [Block Time Out](#) period.
- Bit 1-0: Lighting Mode
 - 00: On/Off
 - 01: Varied PWM
 - 10: Fixed PWM
 - 11: Pulse

9.10.5 Active Sample Period Adjustment

Active Sample Period Adjustment (0xD4)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	Active Sample Period Adjustment							

- Bit 7-0: The sample period of the PIR/Inductive sensor in cycles when the device is in active mode, i.e., when the load is active.

The designer may select 1 of 4 possible sample frequencies as shown in Table 9-2. The frequency selected should be the same as selected in register 0xD5.

Table 9-2: Sampling Frequency Select

Frequency	Register 0xD4 (Decimal)
10 Hz	6
20 Hz	2
50 Hz	1
100 Hz	0



9.10.6 Sample Period

Sample Period (0xD5)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	Sample Period							

- Bit 7-0: Sample Period

The designer may select 1 of 4 possible sample frequencies as shown in Table 9-3. The frequency selected should be the same as selected in register 0xD4.

Table 9-3: Sampling Frequency Select

Frequency	Register 0xD5 (Decimal)
10 Hz	30
20 Hz	11
50 Hz	6
100 Hz	4

9.10.7 I²C Time Out

I ² C Time Out (0xD7)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	I ² C Time Out							

- Bit 7-0: I²C Time Out (0-255)

9.10.8 Light Time Out

Light Time Out (0xD8)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	Light Time Out							

- Bit 7-0: The duration the event LED will remain active in 8ms ticks ((0-255) x 8 ms), as well as the duration of the output pulse (if the pulse UI is selected).

9.10.9 PIR Trigger Time Out

PIR Trigger Time Out (0xD9)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	PIR Trigger Time Out							

- Bit 7-0: The amount of time to clear the PIR Trigger flag in 4.2 second increments ((1-255) x 4.2 sec). The output will be active during this time.

9.10.10 PWM Duty Cycle

PWM Duty Cycle(0xF8)								
Bit Number	7	6	5	4	3	2	1	0
Data Access	Read/Write							
Name	PWM Duty Cycle							

- Bit 7-0: PWM Duty Cycle (1-255)

$$\text{Duty cycle}[\%] = \frac{\text{PWM Duty Cycle}}{255}$$



10 Electrical characteristics

10.1 Absolute Maximum Specifications

The following absolute maximum parameters are specified for the device:
Exceeding these maximum specifications may cause damage to the device.

Table 10-1: Absolute maximum specification

Parameter	Absolute maximum
Operating temperature	-20°C to 85°C
Supply Voltage (VDDHI – GND)	1.8V - 3.6V
Maximum pin voltage	VDDHI + 0.5V (may not exceed VDDHI max)
Maximum continuous current (for specific Pins)	10mA
Minimum pin voltage	GND - 0.5V
Minimum power-on slope	100V/s
ESD protection	±6kV (Human body model)

10.2 Voltage regulation specifications

Table 10-2 Internal regulator operating conditions

Description	Chipset	Parameter	MIN	TYPICAL	MAX	UNIT
Supply Voltage	IQS680	V _{DDHI}	1.8	-	3.6	V
Internal Voltage Regulator		V _{REG}	1.63	1.66	1.69	V

10.3 Power On-reset/Brown out

Table 10-3: Power on-reset and brown out detection specifications

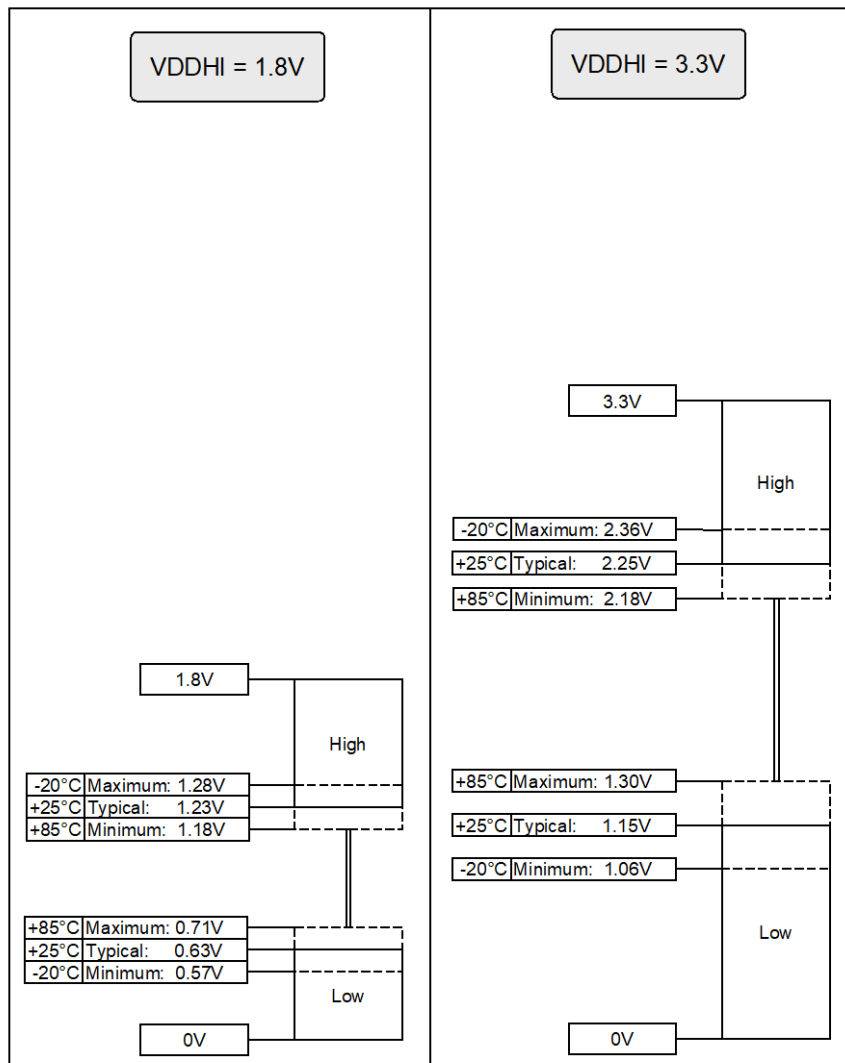
DESCRIPTION	CONDITIONS	PARAMETER	MIN	MAX	UNIT
Power On Reset	V _{DDHI} Slope ≥ 100V/s @25°C	POR	1.15	1.60	V
Brown Out Detect	V _{DDHI} Slope ≥ 100V/s @25°C	BOD	1.20	1.60	V



10.4 Digital input/output trigger levels

Table 10-4 Digital input/output trigger level specifications

DESCRIPTION	Conditions	PARAMETER	Temperature	MIN	TYP	MAX	UNIT
Input low level voltage	400kHz I ² C clock frequency	V _{in_LOW}	-20°C	32.12			% of VDDHI
			+25°C		34.84		
			+85°C			39.39	
Input high level voltage		V _{in_HIGH}	-20°C			71.51	
			+25°C		68.18		
			+85°C	66.06			
Output low level voltage		V _{out_LOW}	-20°C – +85°C		0		
Output high level voltage		V _{out_HIGH}	-20°C – +85°C		100		





10.5 Current consumptions

10.5.1 IC subsystems

Table 10-5: IC subsystem current consumption

Description	TYPICAL	MAX	UNIT
Core active	339	377	μA
Core sleep	0.63	1	μA

10.5.2 PIR and capacitive sensing

Table 10-6: PIR and capacitive sensing current consumption

Power mode	Conditions	Report rate	TYPICAL	UNIT
Active	VDD = 1.8V	10Hz	95.5	μA
		20Hz	97.0	μA
		50Hz	99.3	μA
		100Hz	99.5	μA
Low Power		10Hz	22.4	μA
		20Hz	31.3	μA
		50Hz	43.4	μA
		100Hz	57.4	μA
Active	VDD = 3.3V	10Hz	96.5	μA
		20Hz	98.0	μA
		50Hz	99.8	μA
		100Hz	105	μA
Low Power		10Hz	23.3	μA
		20Hz	32.2	μA
		50Hz	44.1	μA
		100Hz	58.0	μA



10.5.3 Inductive sensing

Table 10-7: Inductive sensing current consumption

Power mode	Conditions	Report rate	TYPICAL	UNIT
Active	VDD = 1.8V	10Hz	114	μA
		20Hz		
		50Hz		
		100Hz		
Low Power		10Hz	23.9	μA
		20Hz	35.2	μA
		50Hz	49.7	μA
		100Hz	67.1	μA
Active	VDD = 3.3V	10Hz	115	μA
		20Hz		
		50Hz		
		100Hz		
Low Power		10Hz	24.9	μA
		20Hz	35.9	μA
		50Hz	50.5	μA
		100Hz	68.9	μA

11 Package information

11.1 DFN10 package and footprint specifications

Table 11-1: DFN-10 Package dimensions (bottom)

Dimension	[mm]
A	3 ±0.1
B	0.5
C	0.25
D	n/a
F	3 ±0.1
L	0.4
P	2.4
Q	1.65

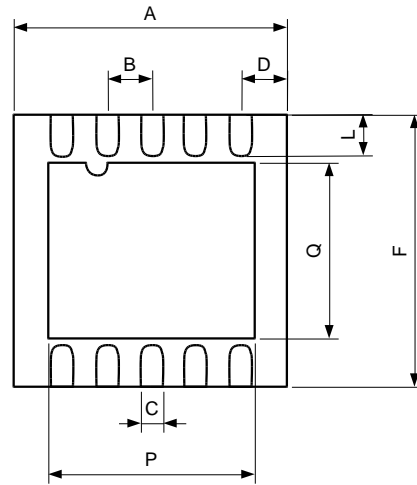


Figure 11.2: DFN-10 Package dimensions (bottom). Note that the saddle needs to be connected to GND on the PCB.

Table 11-2: DFN-10 Package dimensions (side)

Dimension	[mm]
G	0.05
H	0.65
I	0.7-0.8

Table 11-3: DFN-10 Landing dimensions

Dimension	[mm]
A	2.4
B	1.65
C	0.8
D	0.5
E	0.3
F	3.2

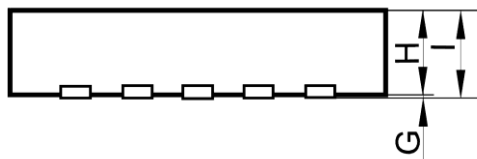


Figure 11.1: DFN-10 Package dimensions (side)

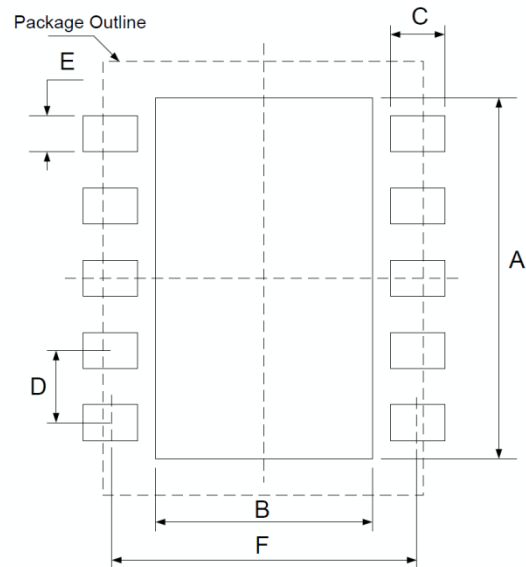
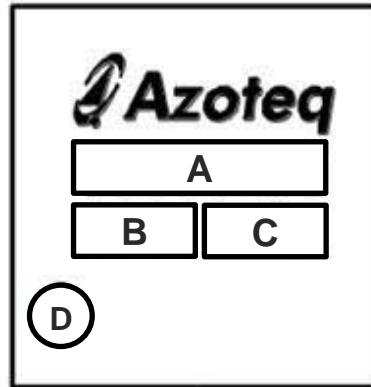


Figure 11.3: DFN-10 Landing dimensions



11.2 Device Marking and ordering information

11.2.1 Device marking:



IQS680 zt xyy PWWYY
A B C

- A. Device name: IQS680-zt
z – IC revision number
t – Temperature range: i (-20° to 85°C)
- B. x – Version
1: Standalone version
2: I2C version
yy – Config⁽¹⁾
00: 44H sub-address
01: 45H sub-address
- C. Batch Number: P
Date code: WWYY
- D. Pin 1: Dot

Notes:

⁽¹⁾ Other sub-addresses available on special request, see Section 7.5.

11.2.2 Ordering Information:

IQS680-xyppb

- x – Version
1 or 2
- yy – Config
00 or 01
- pp – Package type
DN (DFN (3x3)-10)
- b – Bulk packaging
R (3k per reel, MOQ=1 Reel)

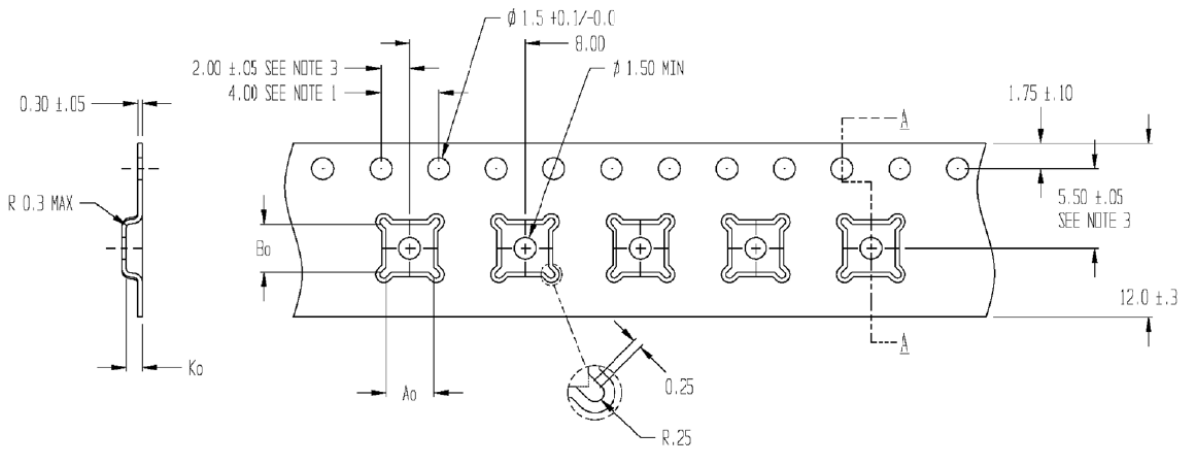
Example:

IQS680-100DNR

- 1 - refers to standalone version
- 00 - config is default (44H sub-address)
- DN - DFN(3x3)-10 package
- R - packaged in Reels of 3k (has to be ordered in multiples of 3k)



11.3 Tape and reel specification

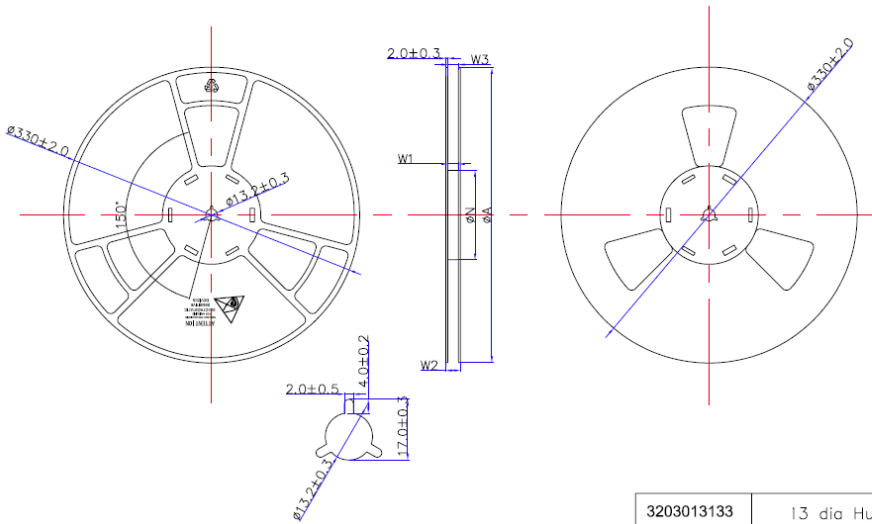


SECTION A - A

A0=3.30
B0=3.30
K0=1.10

NOTES:

- 1、 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ± 0.2
- 2、 CAMBER IN COMPLIANCE WITH EIA 481
- 3、 POCKET POSITION RELATIVE TO SPROCKET HOLE
MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE



PRODUCT SPECIFICATIONS					
TYPE WIDTH	φA	φN	W1 (Min)	W2 (Max)	W3 (Max)
12MM	330 ± 2.0	100 ± 1.0	12.4	18.4	15.4
16mm	330 ± 2.0	100 ± 1.0	16.4	22.4	19.4
24MM	330 ± 2.0	100 ± 1.0	24.4	30.4	27.4

3203013133	13 dia Hub4 12mm width PS B
3203013213	13 dia Hub4 16mm width PS B
3203013253	13 dia Hub4 24mm width PS B



11.4 MSL Level

Moisture Sensitivity Level (MSL) relates to the packaging and handling precautions for some semiconductors. The MSL is an electronic standard for the time period in which a moisture sensitive device can be exposed to ambient room conditions (approximately 30°C/85%RH see J-STD033C for more info) before reflow occur.

Package	Level (duration)
DFN(3x3)-10	MSL 1 (Unlimited at ≤30 °C/85% RH) Reflow profile peak temperature < 260 °C for < 25 seconds Number of Reflow ≤ 3



12 Datasheet revisions

12.1 Revision history

v0.10 – Preliminary structure

v1.00 – Preliminary datasheet

v1.01 – Corrected contact information

v1.02 – Populated current consumption tables

v1.03 – Updated: Reference Schematic

Corrected: Sensor Channel allocation

Added: Device clock, power management and mode operation

Communication

IQS680 Memory Map

V1.04 – Updated: IQS680 Memory Map

V1.05 – Added: Additional OTP options

Writing to EEPROM

Appendix A: EEPROM Sample Code

Updated: Reference Schematic

V1.06 – Updated: IQS680 Memory Map Descriptions

Reference Schematic

Operating Temperature

Added: PWM Duty Cycle Register

V1.07 – Updated: IQS680 Memory Map

Table 8-1

Chapter 5, User Configurable Settings

Chapter 6.3

V1.08 – Updated: IQS680 Memory Map

Reference Schematic

Added: Ordering information

Digital input/output trigger levels

V1.09 – Updated: EEPROM Structure

12.2 Errata



13 Contact Information

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info@azoteq.com



14 Appendices

14.1 Appendix A: EEPROM Sample Code

```
int main(void)
{
    enter_TM();
    write_EEPROM();
    exit_TM();
}

void enter_TM(void)
{
    uint8_t tm_data_0;

    do
    {
        i2c_start();
        i2c_read_register(I2C_IQS680_ADDR, 0x0F,
        &tm_data_0, 1);

        }while( (tm_data_0 != 0xA5));
    }

void write_EEPROM(void)
{
    uint8_t fg_data;
    uint8_t tm_data_1;

    //Read I2C Floating gate
    i2c_start();
    res |= i2c_read_register(I2C_IQS680_ADDR, 0x13 ,
    &fg_data, 1);

    //Enable EEPROM write
    do
    {
        i2c_repeat_start();
        res |= i2c_read_register(I2C_IQS680_ADDR, 0xE4,
        &tm_data_1, 1);
        i2c_stop();

    }while( (tm_data_1 != 0xA6));

    Delay(10); //

    //Write Page 0 to EEPROM
    temp[0] = 0x00;
    temp[1] = 0x2B;
    temp[2] = 0x13;
    #ifndef I2C_MODE
        temp[3] = fg_data | 0x02;
    #else //Standalone mode
        temp[3] = fg_data & 0xFD;
    #endif
    temp[4] = 0xE8;
    temp[5] = CH0_COMPENSATON;
    temp[6] = 0xE9;
    temp[7] = CH1_COMPENSATON;
    temp[8] = 0xEA;
    temp[9] = CH2_COMPENSATON;
    temp[10] = 0xF0;
    temp[11] = CH0_MULTIPLIERS;
    temp[12] = 0xF1;
    temp[13] = CH1_MULTIPLIERS;
    temp[14] = 0xF2;
    temp[15] = CH2_MULTIPLIERS;

    i2c_start();
    res |= i2c_write_register(I2C_E2_ADDR, 0x00 ,
    &temp[0], 16);
    i2c_stop();

    Delay(10); // Allow 10 ms for EEPROM to store data

    //Write Page 1 to EEPROM
    temp[0] = 0x7D;
    temp[1] = CH0_ATI_THRESHOLD;
    temp[2] = 0x7E;
    temp[3] = CH1_ATI_THRESHOLD
    temp[4] = 0x7F;
    temp[5] = CH2_ATI_THRESHOLD;
    temp[6] = 0xF3;
    temp[7] = PXS_SETTINGS_0_0;
    temp[8] = 0xF4;
    temp[9] = PXS_SETTINGS_0_1;
    temp[10] = 0xF5;
    temp[11] = PXS_SETTINGS_0_2;
    temp[12] = 0xF6;
    temp[13] = PXS_SETTINGS_1;
    temp[14] = 0xF7;
    temp[15] = PXS_SETTINGS_2_0;

    i2c_start();
    res |= i2c_write_register(I2C_E2_ADDR, 0x10 ,
    &temp[0], 16);
    i2c_stop();

    Delay(10);

    //Write Page 2 to EEPROM
    temp[0] = 0xF8;
    temp[1] = PXS_SETTINGS_2_1;
    temp[2] = 0xF9;
    temp[3] = PXS_SETTINGS_2_2;
    temp[4] = 0xFA;
    temp[5] = PXS_SETTINGS_3;
    temp[6] = 0x98;
    temp[7] = PROX_THRESHOLD_CH0;
    temp[8] = 0x99;
    temp[9] = TOUCH_THRESHOLD_CH0;
    temp[10] = 0x9A;
    temp[11] = STABLE_THRESHOLD_CH0;
    temp[12] = 0xFB;
    temp[13] = PROX_HALT_TIME;
    temp[14] = 0xFC;
    temp[15] = TOUCH_HALT_TIME;

    i2c_start();
    res |= i2c_write_register(I2C_E2_ADDR, 0x20,
    &temp[0], 16);
    i2c_stop();

    HAL_Delay(10);

    //Write Page 3 to EEPROM
    temp[0] = 0xC8;
    temp[1] = PIR_SETTINGS;
    temp[2] = 0xC9;
    temp[3] = PIR_ENTER_EVENT_THRESHOLD;
    temp[4] = 0xCA;
    temp[5] = PIR_EXIT_EVENT_THRESHOLD;
    temp[6] = 0x5F;
    temp[7] = PIR_THRESHOLD_SCALE_FACTOR;
    temp[8] = 0xBE;
    temp[9] = RE_ATI_TIMEOUT_PIR
    temp[10] = 0xBF;
    temp[11] = BLOCK_TIMEOUT_PIR;
    temp[12] = 0xBC;
    temp[13] = STABILISE_TIMEOUT_PIR;
    temp[14] = 0x1C;
    temp[15] = ACTIVE_CHANNELS;
```



<pre> i2c_start(); res = i2c_write_register(I2C_E2_ADDR, 0x30 , &temp[0], 16); i2c_stop(); Delay(10); //Write Page 4 to EEPROM temp[0] = 0x17; temp[1] = SYST_SETTINGS_0; temp[2] = 0x18; temp[3] = SYST_SETTINGS_1; temp[4] = 0x16; temp[5] = SAMPLE_PER_ADJ; temp[6] = 0xCB; temp[7] = SAMPLE_PER; temp[8] = 0x57; temp[9] = I2C_TIMEOUT_0; temp[10] = 0xBB; temp[11] = LIGHT_TIMEOUT_0; temp[12] = 0xBD; temp[13] = PIR_TRG_TIMEOUT_0; temp[14] = 0xDF; temp[13] = PWM_DUTY_CYCLE; i2c_start(); res = i2c_write_register(I2C_E2_ADDR, 0x40 , &temp[0], 16); i2c_stop(); //Write Page 5 to EEPROM temp[0] = 0xA8; temp[1] = METAL_ENTER_NM_THRESHOLD; temp[2] = 0xA9; temp[3] = METAL_ENTER_M_THRESHOLD; temp[4] = 0xAA; temp[5] = METAL_EXIT_NM_THRESHOLD; temp[6] = 0xAB; temp[7] = METAL_EXIT_M_THRESHOLD; i2c_start(); res = i2c_write_register(I2C_E2_ADDR, 0x50 , &temp[0], 8); i2c_stop(); Delay(10); } void exit_TM(void) { //Write to any register to exit TM i2c_start(); res = i2c_write_register(I2C_IQS680_ADDR, 0xFF, &temp[0], 1); i2c_stop(); } #ifdef IQS680_INIT_H #define IQS680_INIT_H #define I2C_IQS680_ADDR 0x44 #define I2C_E2_ADDR 0x50 #define I2C_MODE /* Change the ProxFusion Sensor Settings 0 */ /* Memory Map Position 0x40 - 0x48 */ #define CH0_COMPENSATON 0x00 #define CH1_COMPENSATON 0x00 #define CH2_COMPENSATON 0x00 </pre>	<pre> #define CH0_MULTIPLIERS 0x00 #define CH1_MULTIPLIERS 0x00 #define CH2_MULTIPLIERS 0x00 #define CH0_ATI_THRESHOLD 0x14 #define CH1_ATI_THRESHOLD 0x20 #define CH2_ATI_THRESHOLD 0x0F /* Change the ProxFusion Sensor Settings 1 */ /* Memory Map Position 0x50 - 0x57 */ #define PXS_SETTINGS_0_0 0x01 #define PXS_SETTINGS_0_1 0x92 #define PXS_SETTINGS_0_2 0x00 #define PXS_SETTINGS_1 0x63 #define PXS_SETTINGS_2_0 0x8A #define PXS_SETTINGS_2_1 0x59 #define PXS_SETTINGS_2_2 0x60 #define PXS_SETTINGS_3 0x05 /* Change the ProxFusion UI Settings */ /* Memory Map Position 0x60 - 0x64 */ #define PROX_THRESHOLD_CH0 0x0A #define TOUCH_THRESHOLD_CH0 0x14 #define STABLE_THRESHOLD_CH0 0x01 #define PROX_HALT_TIME 0x10 #define TOUCH_HALT_TIME 0x0A /* Change the Inductive UI settings */ /* Memory Map Position 0x90, 0x97 - 0x9A */ #define INDUCTIVE_PROX_THRESHOLD 0x00 #define METAL_ENTER_NM_THRESHOLD 0x06 #define METAL_ENTER_M_THRESHOLD 0x04 #define METAL_EXIT_NM_THRESHOLD 0x04 #define METAL_EXIT_M_THRESHOLD 0x06 /* Change the PIR UI settings */ /* Memory Map Position 0x90 - 0x96 */ #define PIR_SETTINGS 0x4B #define PIR_ENTER_EVENT_THRESHOLD 0x01 #define PIR_EXIT_EVENT_THRESHOLD 0x01 #define PIR_THRESHOLD_SCALE_FACTOR 0x10 #define RE_ATI_TIMEOUT_PIR 0x23 #define BLOCK_TIMEOUT_PIR 0x00 #define STABILISE_TIMEOUT_PIR 0x10 /* Change the Device and Power Mode Settings */ /* Memory Map Position 0xD0 - 0xD9 */ #define I2C_COMMAND 0x00 #define ACTIVE_CHANNELS 0x83 #define SYSTEM_SETTINGS_0 0x44 #define SYSTEM_SETTINGS_1 0x80 #define ACTIVE_SAMPLE_PERIOD_ADJUSTMENT 0x00 #define SAMPLE_PERIOD 0x04 #define PERIOD_COUNTER 0x00 #define I2C_TIMEOUT 0x06 #define LIGHT_TIMEOUT 0x00 #define PIR_TRIGGER_TIMEOUT 0x01 /* Change the PWM Value */ /* Memory Map Position 0xF8 */ #define PWM_DUTY_CYCLE 0xFF </pre>
---	---